Two Stage CMOS Operational Amplifier

From Specification to Design

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Abstract: *The goal of this report to describe the design of a CMOS operational amplifier, which is designed to meet certain given specifications. Based on a clear understanding of the specs, the circuit topology of the standard CMOS operational amplifier was chosen because it was believed that such a design could meet the specs and that the design of such an amplifier is fairly simple. Comparison is drawn between given specifications and result from computer simulations using hspice in the schematic level. Here we had taken 0.25um model from TSMC. The results are noted to be satisfactory.*

Introduction

Operational Amplifier is the most common building blocks of most of the electronics system may not need introduction. They are integral part of many analog and mixed signal systems. Opamps with vastly different level of complexity are used to realize functions ranging from dc bias generation to high gain amplification, filtering or ADCs. The design of opamp continues to pose a challenge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technology.

Opamp consists of one or more differential stages and usually followed by additional gain stages depending upon the requirements. Here we discuss regarding the design of two-stage cmos opamp. The paper consists of understanding of specifications and circuit topology of opamp. Design procedures along with one example of opamp design using tsmc 0.25 um technology with single bias supply 2.5V is also given. Finally the simulation results of hspice simulator with comparison of specifications of opamp are given. We met all of the specifications of opamp!!!

Specifications of opamp

The design starts with the understanding of the specifications. Some common definitions of operational amplifier specifications are given below. The design specs is given in table no 1.

Open Loop Gain: It is the ratio between output voltage and differential input voltage. Because the output signal is much larger than the input signal, so it is commonly called as large signal voltage gain.
Slew Rate: The maximum rate of change of output voltage per unit time. (dVo/dt) The slope of the out put signal is the slew rate.
Rise time : the time required by the output to go from 10% to 90% of its final value is called the rise time.
Overshoot: The maximum amount by which the output deviates form its steady state value is the overshoot.

CMRR: Common Mode Rejection ratio is the ratio between differential gain and common mode gain.
Power Dissipation: The amount of power dissipated. It is the product of voltage and total current in the circuit.

Circuit Operation

The final circuit designed to meet the required specifications is shown in Figure 1. The topology of this circuit is that of a standard CMOS op-amp. It comprised of three subsections of circuits, namely differential gain stage, second gain stage and bias strings.. it was found that this topology was able to successfully meet all of the design specifications. Examining the subsections further will provide valuable insight into the operation of this amplifier.

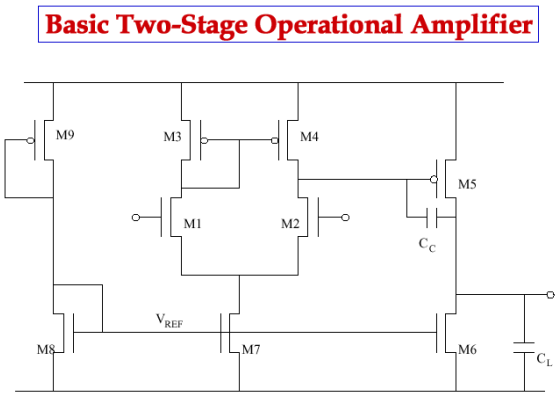

Figure 1: Two stage operational amplifier

Differential Gain Stage

The first subsection of interest is the differential gain stage which is comprised of transistors M1 through M4. Transistors M1 and M2 are standard N channel MOSFET (NMOS) transistors which form the basic input stage of the amplifier. The gate of M1 is the inverting input and the gate of M2 is the non-inverting input. A differential input signal applied across the two input terminals will be amplified according to the gain of the differential stage. The gain of the stage is simply the transconductance of M2 times the total output resistance seen at the drain of M2. The two main resistances that contribute to the output resistance are that of the input transistors themselves and also the output resistance of the active load transistors, M3 and M4. The current mirror active load used in this circuit has three distinct advantages. First, the use of active load devices creates a large output resistance in a relatively small amount of die area. The current mirror topology performs the differential to single-ended conversion of the input signal, and finally, the load also helps with common mode rejection ratio.

Second Gain Stage

The purpose of the second gain stage, as the name implies, is to provide additional gain in the amplifier. Consisting of transistors M5 and M6, this stage takes the output from the drain of M2 and amplifies it through M5 which is in the standard common source configuration. Again, similar to the differential gain stage, this stage employs an active device, M6, to serve as the load resistance for M5. The gain of this stage is the transconductance of M5 times the effective load resistance comprised of the output resistances of M5 and M6.

Bias String

The biasing of the operational amplifier is achieved with only four transistors. Transistors M8 and M9 form a simple current mirror bias string that supplies a voltage between the gate and source of M7 and M6. Transistors M6 and M7 sink a certain amount of current based on their gate to source voltage which is controlled by the bias string. M8 and M9 are diode connected to ensure they operate in the saturation region. Proper biasing of the other transistors in the circuit (M1 – M5) is controlled by the node voltages present in the circuit itself. Most importantly, M5 is biased by the gate to source voltage (VGS) set up by the VGS of the current mirror load as are the transistors M1 and M2.

Design of the OpAmp

The first aspect considered in the design was the specifications to be met. They appear in Table 1 of this report. Based on a clear understanding of the specs, the circuit topology of the standard CMOS operational amplifier was chosen because it was believed that such a design could meet the specs and that the design of such an amplifier is fairly simple.

Procedure

The schematic of the opamp is given in figure 1. We adopted a common procedure to design the opamp, which is already available in any book of the analog integrated circuit.. One example for designing the opamp with tsmc 0.25um technology is also given. The procedures are given below

1. Chose I6 to be as a value which will be decided by slew rate and power dissipation.
2. Find the value of compensation capacitor Cc= I6/Slew Rate
3. Find gm1 from gain bandwidth=gm1/2π*Cc
4. Find gm5 from condition of stability gm5~2.2*gm1
5. Gain Av = {g m1 g m5 } / { (g ds2 + g ds4) (g ds5 + g ds7) }
   = {gm1*gm5 } / { (λ2 + λ4)I DS2 (λ5 + λ7)I 7 }
6. Calculate I7 > (C C + C L) SR
7. Find out I7 from steps 5 and 6
8. Find (W/L)1,2 from (g m = SqRt{ 2 K (W/ L)I DS })
9. Then (W/ L)5 from (W/L = g m /{ 2 K * I DS })
10. M3, M4 are matched devices.For matching of the mirror voltages V DS3 = V DS4 And since V GS3 = V DS3 and V DS4 = V GS5 then V GS3 = V GS5
    $(W/L)_3 = (W/L)_5 * I_{DS3} / I_{DS5}$
11. The W/L ratio of current sinks M6 and M7 can be found from common cureent equation of the mosfet.
12. M8 and M9 is bias strings of opamp

Example:

Specifications of opamp (See table no 1)

Gain=30,000
Gain Bandwidth=10MHz
Slew rate = 20V/us

For TSMC 0.25um technology
$Kn = \mu_n * Cox \sim 135uA/V^2$
$Kp = \mu_p * Cox \sim 45uA/V^2$

The sizes of the transistors are calculated by using the above steps.

1. I6=50uA
2. Cc=2.5PF
3. Gm1=502ua/V
4. Gm5= 1074ua/v
5. I7< 590uA
6. I7> 225uA
7. I7 ~ 500uA
8. W/L)1,2 = 31
9. W/L)5 = 20
10. W/L)3,4 = 1.5
11. W/L)6 =2.5
12. W/L)7 =27

Troubleshooting

Once you had fixed the width and length of the device, check all transistors should be in saturation. Check the dynamic range of the differential amplifier through dc simulation. Try to optimize for more linearity at the output. Here we had taken bias supply is 2.5V, so the output swing from 0 to 2.5V. This can be optimized by changing the output impedance of the (M1, M2), and (M3, M4). Fix the input dc voltage for which the output swings maximum value. Check the dc voltage of the output differential stage. Then apply the same voltage to the input of the succeeding stage, and optimize the transistor sizes of the output stage for getting maximum swing.

With this optimized condition we simulate the circuit. The result of the simulation does not meet the specs of the opamp. So we fix the specs of opamp with computer iterations, which are discussed below.

Fixing the Gain

With the voltage bias being provided by a constant 1.25 V dc source, the circuit was now simulated to check for any errors in computation and to see if the gain specification was met. When simulated, the gain was low by 500 So an increase in the gain was achieved by increasing the width of the input transistors M1 and M2 to 40um This raised the gain to 30300, which is our required specifications. The first specs were met.

Unity Gain, Phase Margin & Slew Rate

The next specification to achieve was that of the unity gain frequency. Based on the equation for setting the dominant pole using a compensating capacitor, the compensating capacitor was calculated to be 4.5 pF. A problem became clear; with this low of a capacitor and such a large load capacitance, the poles and zeros of this amplifier were not far apart, and the phase margin was questionable. At this point the circuit was again simulated using a constant dc biasing source. The simulation showed that the unity gain frequency was too low; the GB needed to be raised. To raise GB by decreasing Cc would further reduce the phase margin because the pole splitting ability of Cc would be

reduced. A combination of raising gm2 and decreasing Cc was chosen to most effectively achieve a higher unity gain frequency. This was accomplished by a few simulation iterations of raising the bias voltage to increase the current through M2 and thus raise its transconductance. However, the current could only be raised so far before it started to degrade the gain. In the end, the current through M2 was raised slightly and the compensating capacitance was reduced slightly.

The phase margin was checked on the simulation and found to be 42 degrees. Such a low value of phase margin will degrade the settling time of the op-amp. Based on the design, however, to meet the gain and unity gain frequency specifications not much could be done about increasing the phase margin without changing the topology of the circuit.

Then the slew rate was measured. It is 17.8 V/us against the specs 20 V/us. The slew rate is given by

$$SR = \frac{(Id6 - Id7)}{Cc + CL}$$

So increasing the drain current can increase the slew rate, but it will increase the power dissipation. If we reduce the compensating capacitor, the phase margin will be poor. So this value of slew rate would be acceptable.

Bias String

Running the simulations with a constant dc voltage source as the voltage bias allowed the design to quickly be changed and tweaked until the proper specs were met. It was found that, the final simulated out put needs the bias voltage (VGS7) was 1.1 V. And drain current is 25uAFirst the VGS8 was set to 1.1 V and the bias current of 25 uA. Then, solving the MOSFET current equation we get W/L ratio for M8 and M9 transistors. W/L of 8 is calculated 1 and that of M9 is 9

The final bias string was added to the spice netlist and a simulation was run. The VGS7 that the bias string produced was too low so the ratio of M8 was raised and the ratio of M9 was lowered until the proper VGS7 was achieved. With all transistors in place and a finalized design, the test suite was run again, and the results were verified with the given specifications to make sure the op-amp performed to spec. All specifications were met!!!

Simulation and Results

Verification of the design was performed using the circuit simulator *Avanti Star-Hspice 99.2*. The netlist is given below that corresponds to Figure 1, which was entered into the simulator Various circuit configurations were used to verify the achievement of the specifications of this design. All the simulated results with comparison of the specs of opamp is given in table 1.

NETLIST OF TWO STAGE CMOS OPERATIONAL AMPLIFIER

```
Vbias vdd 0  dc=2.5
M9 net47 net47 vdd vdd pch w=5u l=2u
M8 (net47 net47 0 0) nch w=3.5u l=2u
M7 (net55 net47 0 0) nch w=3.5u l=2u

* DIFFERENTIAL INPUT THROGH Vp and Vn
M2 (net53 Vp net55 0) nch w=60u l=1.15u
M1 (net56 Vn net55 0) nch w=60u l=1.15u

* OUT PUT OF THE OPAMP IS THROUGH VOUT
M5 (Vout net53 vdd vdd) pch w=100u l=1u
M6 (Vout net47 0 0) nch w=32.5u l=1u
M3 (net53 net56 vdd vdd) pch w=6u l=2u
M4 (net56 net56 vdd vdd) pch w=6u l=2u
* CL IS LOAD CAPACITOR AND CC IS COMPENSATING CAPACITOR
CL (Vout 0)  20p
CC (net53 Vout) 4p
.end
```

RESULTS AND DISCUSSIONS

The following sections discuss the simulations and their results. The table 1 shows the simulated output of the opamp.

TABLE 1: SPECIFICATIONS OF OPAMP (With Load Capacitor 20pF)

PARAMETER	**SPECIFICATIONS**	**RESULTS ACHIEVED**
GAIN	30,000	32,000
GAIN BAND WIDTH	10MHz	11.8 MHz
SETTLING TIME	200NS	150NS
OVERSHOOT	6%	4%
TOTAL POWER DISSIPATION	< 2mW	1.96mW
RISE TIME	250NS	80NS
CMRR	80dB	84dB
SLEW RATE	20V/Us	17.8 V/uS

Performance Specifications

Each specification was tested to verify that the designed amplifier met the specifications. The results of these tests appear below in Table 1. Note that the simulation results are compared with the specs value of the op-amp. All simulations had good agreement with the opamp specs except for the slew rate. This may be due to low power dissipation.

Simulation Discussion

The simulation results show that this op-amp performed to within specs for all the specified parameters. What follows is a brief discussion of each parameter. The use of the standard CMOS op-amp topology had both advantages and disadvantages for achieving the desired specifications. As reported however, this topology was able to meet all the desired specifications.

One of the main advantages of the standard topology CMOS amplifier is the large gain it can achieve. The two gain stages obtain the large single gain. The open loop gain of the opamp was measured using avanwaves to view the simulation result of hspice. The graph is shown in figure 2.

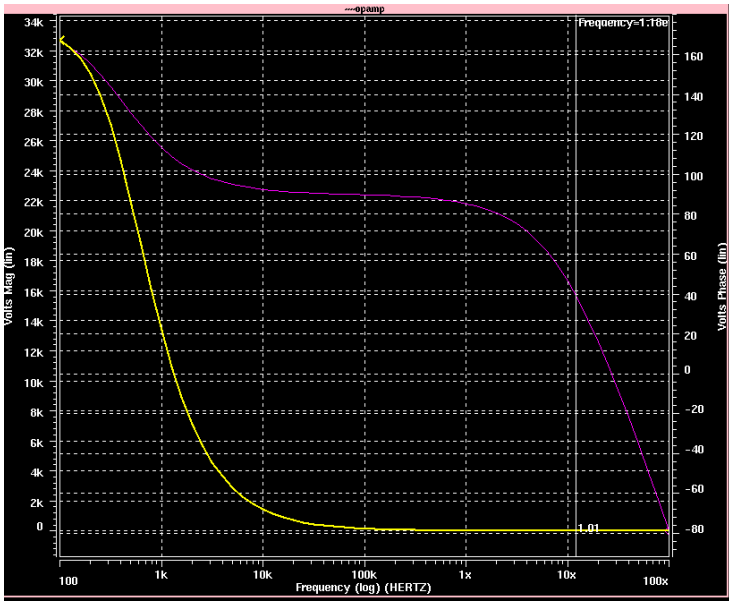

Figure 2 Graph between frequency and gain and phase

The slew rate of the standard CMOS operational amplifier in this design was affected by two different parameters. Both the phase margin and the out put drain current. slew rate of the amplifier will alter the settling time. The slew rate of the standard op-amp is adequate for achieving the specification of settling time in this design. We get a slew rate of 17.8 V/uS against the specs 20V/uS. The slew rate could have been increased, but it was limited due to the amount of current that was allowed by the power dissipation spec.

Conclusion

This design of opamp is one part of IP development work in RF & analog group. The design of two-stage cmos operational amplifier is described in this paper. The simulation results showing that the design meets all the specs except the slew rate. This slight low value (10 % less) of slew rate may be due to low current chosen to meet low power dissipation. (<2mW). However one can achieve better performance opamp by sacrificing some other parameter. The results achieved in this design work may be noted to be satisfactory.