DESIGN OF ZIGBEE RF FRONT END IC IN 2.4 GHz ISM BAND

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Outline

- Introduction to ZigBee
- Objectives
- Motivation
- Block Diagram
- Specifications
- Methodology
Introduction to ZigBee

- Based on IEEE 802.15.4 standard
- Supports 3 operating bands-
  - 868 MHz for Europe,
  - 915 MHz for US,
  - 2.4 GHz for the rest of the world
- IEEE 802.15.4 defines the radio physical and MAC layers whereas ZigBee defines the network, security and application frameworks for an IEEE 802.15.4-based system
- Suitable for simpler and less expensive wireless personal area networks
Objectives

To design, integrate and analyse the following components to fabricate a RF Front End IC for ZigBee applications in 180nm:

- Transmitter path consisting of the Power Amplifier (PA).
- Receiver path consisting of the Low Noise Amplifier (LNA).
- Switching circuitry to select transmit and receive paths.
- The associated matching networks.
- The harmonic filter.
Motivation

- Development of IoT: need for low cost and low power device for wireless communication
- Applications of ZigBee:
  - Energy Management and Efficiency.
  - Home Automation.
  - Building Automation.
  - Industrial Automation.
  - Bio-Medical Applications.
Methodology

Understanding the specifications of RF transmitter and receiver

Literature survey

Theoretical comparison of architectures for implementing RF transmitter and receiver

Design of the blocks on paper for LNA, PA, switching circuitry, matching network & harmonic filter

Cadence design simulation for individual blocks and integrating them

Layout of the design

DRC check for the design

LVS check

Post extraction simulation

Converting design to GDSII for fabrication
# Specifications

## Transmitter Path Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Operating Frequency Band</td>
<td>2.4 GHz to 2.5 GHz</td>
</tr>
<tr>
<td>Output P1dB</td>
<td>18 dBm</td>
</tr>
<tr>
<td>Saturated Output Power</td>
<td>20 dBm</td>
</tr>
<tr>
<td>Small Signal Gain</td>
<td>24 dB</td>
</tr>
<tr>
<td>Input/Output Impedance</td>
<td>50 ohm</td>
</tr>
<tr>
<td>TX Quiescent Current</td>
<td>18 mA</td>
</tr>
<tr>
<td>TX High Power Current</td>
<td>90 mA</td>
</tr>
</tbody>
</table>

## Receiver Path Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Operating Frequency Band</td>
<td>2.4 GHz to 2.5 GHz</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>2.5 dB</td>
</tr>
<tr>
<td>Gain</td>
<td>12 dB</td>
</tr>
<tr>
<td>Input P1dB</td>
<td>-10 dBm</td>
</tr>
<tr>
<td>Input/Output Return loss</td>
<td>12 dB</td>
</tr>
<tr>
<td>RX Quiescent Current</td>
<td>10 mA</td>
</tr>
<tr>
<td>RF Port Impedance</td>
<td>50 ohm</td>
</tr>
</tbody>
</table>
# Extra Information

## Academic Pricing

<table>
<thead>
<tr>
<th>Prototype Manufacturing Technology through CMC</th>
<th>Prices</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Canadian Academic Peer-Reviewed Price</td>
<td>Canadian Academic Price</td>
</tr>
<tr>
<td></td>
<td>$/mm²</td>
<td>$/mm²</td>
</tr>
<tr>
<td><strong>Microelectronics</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ATMicroelectronics 20nm CMOS FD SOI (through CMP)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$4,000</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$12,000</td>
</tr>
<tr>
<td></td>
<td></td>
<td>See Fab Schedule To Apply</td>
</tr>
<tr>
<td>TSMC 65nm CMOS GP (through MOSIS)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$2,250</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$9,950</td>
</tr>
<tr>
<td></td>
<td></td>
<td>See Fab Schedule To Apply</td>
</tr>
<tr>
<td>TSMC 65nm CMOS LP (through MOSIS)</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>TSMC 65nm CMOS (through MOSIS) - CRN600</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>GF (IBM) 13nm CMOS (through MOSIS): CMOSP13</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$900</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$2,000</td>
</tr>
<tr>
<td></td>
<td></td>
<td>See Fab Schedule To Apply</td>
</tr>
<tr>
<td>TSMC 0.15µm CMOS (through MOSIS) - CMOSP19</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$500</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$1,425</td>
</tr>
<tr>
<td></td>
<td></td>
<td>See Fab Schedule To Apply</td>
</tr>
<tr>
<td>TSMC 0.35µm CMOS (through MOSIS) - CMOSP35</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$200</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$525</td>
</tr>
<tr>
<td></td>
<td></td>
<td>See Fab Schedule To Apply</td>
</tr>
<tr>
<td>AMS 0.15µm CMOS - Standard (through CMP): AMSP35</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$225</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$1,000</td>
</tr>
<tr>
<td></td>
<td></td>
<td>See Fab Schedule To Apply</td>
</tr>
<tr>
<td>AMS 0.15µm CMOS - Opto (through CMP): AMSP35</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$225</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$1,200</td>
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</tbody>
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A 65-nm mask set can cost 1.8 times that of a 90-nm set, while a 45-nm mask set can cost 2.2 times that of a 65-nm set.

- *EE Times 10/7/2010*
CMOS RF INTEGRATED CIRCUITS

- CMOS
  - Cheap & mass produced
- RF
  - Radio’s
- IC
  - About highly integrated things/circuits

Cellphones, Wi-fi, Bluetooth, etc
MOSFET

- Basic structure of MOSFET
- Formation of channel
- Different regions of operation: Cut-off, ohmic and saturation
- Final model of the MOSFET after considering all the capacitances: $C_{gs}$, $C_{gd}$, $C_{gb}$, $C_{sb}$, $C_{db}$; gate resistance, contact resistance, inductance
- Metrics of MOSFET:
  - Transition frequency, $f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$
  - Max frequency, $f_{MAX} = \frac{1}{2} \left( \frac{f_T}{\sqrt{2\pi f_T C_{gd} (R_g + R_s) + \frac{R_g + R_s}{r_o}}} \right)$
BASIC RF TRANSCEIVER

Power received $\alpha \frac{1}{x^2}$
Antenna power received $\alpha$ Area of antenna
PRE-REQUISITES

- RLC
- Distributed Networks
- Elements of an IC
- MOSFETS
Reflection coefficient

\[ Z_S = Z_O \rightarrow \text{No echo's allowed} \]
\[ Z_L = Z_O \rightarrow \text{No reflection} \]

\[ Z_S = Z_O = Z_L \]
- Input of LNA has to be matched to \( Z_O \) of antenna.
- Output of PA has to matched to \( Z_O \) of antenna.
When a wave is launched part of the energy is absorbed by load and part of it is reflected to source, at source, part of it is absorbed and remaining part is reflected back.

\[ \Gamma = \frac{Z - Z_0}{Z + Z_0} \]

Non conducting medium → \( Z_0 = \sqrt{\mu / \varepsilon} \approx \sqrt{\mu_0 / \varepsilon_0} \)

Conducting medium → \( Z_0 = \sqrt{\frac{l'}{c'}} \)

- \( l' \) → inductance per meter
- \( c' \) → cap per meter
As time progresses to infinity, the voltage at source is equal to load and is equal to load to half.

- When load $Z$ is equal to $Z_0$ then no reflection
- When load $Z$ is not equal to $Z_0$ then no reflection
• For no reflection:
  - $Z_{LNAS} = Z_1 = Z_{MIXERL}$

• Typical value of characteristic impedance is:
  - 75Ω – used for cable TV and all kind of T.V.
  - 50Ω – application other then T.V.

• For no reflection:
  - $Z_s = Z_o$ of antenna
TRANSMISSION MEDIA & REFLECTION

• For no reflection:-
  - \( R_L = Z_0 \)
  - \( R_S = Z_0 \)
  - \( R_L = R_S = Z_0 \)

• To get maximum power received means –
  - No reflection
  - \( P_{out} = P_{in} \times \text{Power Gain} \)

• GSM phone has sensitivity of -100dBm=0.1pW which is extremely low. That’s why maximum power transfer is important.
POWER GAIN

- Law of Conservation:
  - $P_{\text{in}} = P_{\text{out}} + P_{\text{wasted}}$
- Power Gain: $\frac{P_{\text{out}}}{P_{\text{in}}}$

- $P_{\text{load}} + P_{\text{wasted}} = P_{\text{signal}} + P_{\text{power supply}}$
- Quality Factor = $(w)(\text{Peak energy stored}) / (\text{average power consumed})$
RLC Network

Parallel RLC

Series RLC

\[ I_L = \frac{IR}{\sqrt{L/C}} \]

\[ I_C = jIR \cdot \frac{1}{\sqrt{L/C}} \]
RLC Circuits

**SERIES RLC**

\[ Q = \frac{1}{\omega_0 RC} = \frac{\omega_0 L}{R} = \frac{1}{R} \sqrt{\frac{L}{C}} \]

**PARALLEL RLC**

\[ Q = R \sqrt{\frac{C}{L}} \]
RLC Circuits

 transient response of RLC circuit for step input

\[ Q(\omega) = \omega \times \frac{\text{Maximum energy stored}}{\text{Power loss}} \]

\[ BW = \Delta f = f_H - f_L = \frac{f_c}{Q} \]

Example:
For GSM system, Center Frequency, \( w_0 \) is 800MHz, channel spacing is 200KHz, calculate the Q factor. Is it possible to make an IC for the following system with the calculated Q?

\[ Q = \frac{w_2 - w_1}{w_0} \]

\( Q = 4000 \). Not Possible, Since in an IC we can achieve maximum upto 10 or 15, above that we have to use discrete components to achieve max of 100.
RLC Circuits

**SERIES RLC**

$R$, $L$, $C$

$V(t)$

$i(t)$

**PARALLEL RLC**

$V_s$

$I_s$

$I_R$, $I_L$, $I_C$

$R_s$, $C_s$, $L_s$

$R_p$, $C_p$

Series-Parallel Transformation

\[ R_p = R_s \left[ 1 + \left( \frac{\omega L_s}{R_s} \right)^2 \right] = R_s (1 + Q_s^2) \]

\[ L_p = L_s \left[ 1 + \left( \frac{R_s}{\omega L_s} \right)^2 \right] = L_s \left( 1 + \frac{1}{Q_s^2} \right) \]

\[ R_p \approx Q_s^2 R_s \]

\[ C_p \approx C_s. \]

\[ R_p = (Q_s^2 + 1) R_s. \]

\[ C_p = \frac{Q_s^2}{Q_s^2 + 1} C_s. \]
Matching Circuits

• Why do we need Matching?
  - Retaining the shape of signal
  - Maximum Power Transfer
  - Avoid Reflections
Matching Circuits

• Matching Topologies:
  - Transformer
  - LC network
    - L-Match
    - \( \pi \)-Match
    - T-Match
    - Tapped L/C Match
Matching Circuits

Transformer

- Ideal Transformers do not exist
- Its not lossless (Cu, Core)

\[
\frac{N_s}{N_p} = \sqrt{\frac{Z_g}{Z_l}}
\]
Matching Circuits

**L-Match**

- Only 2 Degrees of freedom, (L,C)
- Bandwidth limited due to Q

- Compute Q, L, C.
Other Matching Circuits

\[ \Pi \text{-Match} \]

\[ T \text{-Match} \]
Other Matching Circuits

Tapped L/C Match
Other Matching Circuits

Tapped L/C Match
Other Matching Circuits

• Comparision of Matching Networks
PASSIVE DEVICES - does not need power supply

- Examples - R, L, C, M wires, diodes

ACTIVE DEVICES – need power supply.

- Examples - MOS, BJT, JFET etc.

Resistors:

- made up of polysilicon or metal.

\[ A = w \cdot h \]
\[ R = \frac{\rho l}{A} = \frac{(\rho h)}{(l/w)} \]
Capacitor

- Net capacitance, $C = \frac{A \varepsilon}{d}$ + fringing capacitance
- Fringing capacitance $\alpha (\varepsilon/d)$ (perimeter $\times$ height / fuzz factor)
Capacitor on IC:

- Area, Distance, Perimeter is important
- Fringing capacitance is important in normal capacitance when the distance between two plates is comparable than length and width
- With MOSFET, well controlled, high density capacitance is achieved.
Passive IC Components: INDUCTORS

- Inductors resist change in magnetic flux thereby, induce an emf potential to oppose the change.
- Inductance depends on
  \[ L = \frac{1}{l} \mu_0 K N^2 A \]

- Non Idealities:
  - Copper Losses
  - Core Losses

  Amount of power lost in Inductor: \( i^2 x R_{copper} \)

  \[ R_{copper} = L x \frac{p}{w} \]
Passive IC Components: INDUCTORS

- Inductors resist change in magnetic flux thereby, induce an emf potential to oppose the change.
Inductors and Wires

Inductors

- Below resonant frequency, parallel LC N/W acts more like a inductor and above, it acts more like a capacitor

- While doing layout of the inductor
  - The top metal layer can be chosen to reduce the parasitic capacitance
  - The gap between the wires can be increased to reduce the turn-to-turn capacitance
  - The thickness of the wire can be increased to reduce the resistance of the wire

- To reduce Eddy currents
  - Can use the top most metal layer to increase the gap b/w inductor and substrate
  - Can use a more resistive substrate but is limited by the Latch-up problem. So use trenches and blocking mechanism to increase the resistivity
Inductors and Wires

Wires

- Has resistance of $R = \frac{\rho \cdot L}{\pi \cdot R^2 - \pi \cdot (R - d)^2}$ where skin depth, $d = \sqrt{\frac{2}{\mu \cdot \sigma \cdot \omega}}$

- Have Inductance per unit length of, $L' = \frac{\mu}{\pi} \cdot \ln(h/r)$

- Observations:
  - Longer the wire, more the inductance
  - More the separation b/w the wire and substrate, more is the inductance of the wire
Wires

Wire also has capacitance per unit length of \( C' = \frac{w}{h} \varepsilon \left(1 + \frac{1}{K}\right) \)

where \( K \)-fuzz factor

Observations:

- As \( h \) increases, \( C' \) also increases, but \( L' \) decreases
- As \( w \) increases, \( C' \) also increases, but \( L' \) decreases
- Therefore, for any wire \( L' \cdot C' = \) a constant
- The model of the wire at RF frequencies is as shown:
Transmission Lines

- The characteristic impedance of the wire as a function of $R'$, $L'$, $G'$, $C'$ and frequency is

\[
Z_0 = \frac{\sqrt{R' + j\omega L'}}{\sqrt{G' + j\omega C'}}
\]

- If there exists reflections, then the shape of the input signal will be distorted as the signal takes time to settle to its final value.

- Voltage at any point on the wire is the sum of both the forward and backward moving wave

- The reflection coefficient at the load end is given by

\[
Z_o = \frac{Z_L - Z_O}{Z_L + Z_O}
\]

- Reflection coefficient is a function of frequency and hence, it is different for different frequencies
Low Noise Amplifiers

Motivation:

- Noise of a system is greatly influenced by the first stage in a system.
- Increasing gain of the first stage also reduces the overall noise factor.
- Example:

  ![Diagram of stages](image)

  - $N_f$ of system is 2.4 when stage 1 has 10 dB as a gain
  - $N_f$ of system drops is 1.5 when stage 1 has 20 db as a gain
Low Noise Amplifiers

- First stage in the receiver side needs to be an amplifier.
- From the previous study, the first stage needs to have low noise and high gain.
- Hence, the low noise amplifier.
- Requirements of a low noise amplifier:
  - Large Gain
  - Low noise figure
  - Linearity
  - Input and output Matching
Low Noise Amplifiers

Matching at input side:

Consider the following:

- Input at gate side of the Mosfet looks like a capacitor.
- One solution could be to add a resistor at the input, considering the matching network takes care of the capacitance.
Low Noise Amplifiers

Advantages

✓ Input matching is achieved.

✓ Good gain may be achieved.

Disadvantages

➢ Additional $R_s$ contributes to additional noise.

➢ NF is at least 2, i.e., greater than 3dB at least.

➢ Thus, horrible NF even before considering the Mosfet.
Low Noise Amplifiers

Other possible design solutions:

Disadvantages:
1) Channel noise adds up to the noise
2) Depends on $g_m$ of the device.

Disadvantages:
Resistor is used here, and thus adds up to the noise. Use of resistors here is not recommended.

Still, used in some applications like oscilloscopes and active probes.
Low Noise Amplifiers

First cut design:

Analysing using small signal model

\[ Z_{in} = Z + Z \cdot \frac{g_m}{j \omega C_{gs}} + \frac{1}{j \omega C_{gs}} \]
Low Noise Amplifiers

First cut design:

- \( Z \) cannot be a resistor, as we minimise use of resistors due to its contribution to noise.

- \( Z \) cannot be a capacitor as this will result in a negative resistance and would lead to positive feedback circuitry.

- Hence, using \( Z \) as an inductance would be a solution and \( Z_{\text{in}} \) would seem to have a resistive component of \( \text{gm} \cdot (L_s / C_{gs}) \) which won’t generate noise.

- When \( Z \) is used as inductance, the remaining \( L_s \) and \( C_{gs} \) can be tuned out with resonant frequency:

\[
f_0 = \frac{1}{2\pi \sqrt{L_s \cdot C_{gs}}}
\]
Low Noise Amplifiers

Load side:

- Gain here is approximately \( \frac{Load \text{ Impedance}}{Degeneration \text{ Impedance}} \).

- This gain might not be good enough.

- Also, \( C_{gd} \) here can cause instability.

- Hence, cascaded structure can be a good idea.

We also need to make sure that the first drain node needs to be a low impedance node since analysis of input side would change otherwise.
Low Noise Amplifiers

Load side:

- At this point too, impedance matching need to be done to get good gain.

- Impedance looking at load of $M_2$ should be same as impedance looking towards the source side of $M_2$.

- This would then allow a proper matching to transfer the required power and get a desirable gain.
Low Noise Amplifiers

Load side:

- $Z_d$ is like a huge inductance.
- Thus, $Z$ will finally look like large inductance.
- This will be able to drive load capacitances well.
Low Noise Amplifiers

**FINAL LNA DESIGN**

- Matching is achieved here.
- Decent gain is achieved due to cascade stage.
- Noise of the circuit depends on the channel noise of the first stage mosfet.
- The channel noise of the first mosfet depends on the $C_{gs}$ of the device which in turn depends on the device geometry.
- Channel noise of the second mosfet doesn’t play a significant role as it gets divided by the large gain.

Future work includes more insight into other topologies which includes noise cancellation techniques.
Power Amplifiers

- Important parameters of Power Amplifier -
  - Efficiency
  - Linearity

- Generic structure of Power Amplifier -

- Class A Power Amplifier
  - Max Efficiency - 50%
  - Conduction Angle - 100%
Power Amplifiers

- Class B Power Amplifier
  - Max Efficiency: 78.5%
  - Conduction Angle: 50%
Power Amplifiers

- Class C Power Amplifier
  - Max Efficiency: \( \eta = \frac{2\phi - \sin(2\phi)}{4\sin(\phi) - \phi \cos(\phi)} \)
  - Conduction Angle: 50%
Valuable suggestions

Thank You