Power Amplifier

Literature Survey

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P-1: Design of a 2.4GHz Power Amplifier

- ❑ Switch type power amplifier is the most important characteristic of high efficiency.
- ❑ The efficiency of the switch amplifier in turn depends on the gate driving signal.
- ❑ To achieve a suitable gate signal two pseudo E class drivers are implemented.
- ❑ Limited DC RF choke inductance is used.
- ❑ Due to large inductances in this circuit a bond wire is used for testing.
- ❑Supplies high power combined with proper working of power stage at the respective states.
- ❑ Consists of Class F-amplifier, inverter and Class E drivers.

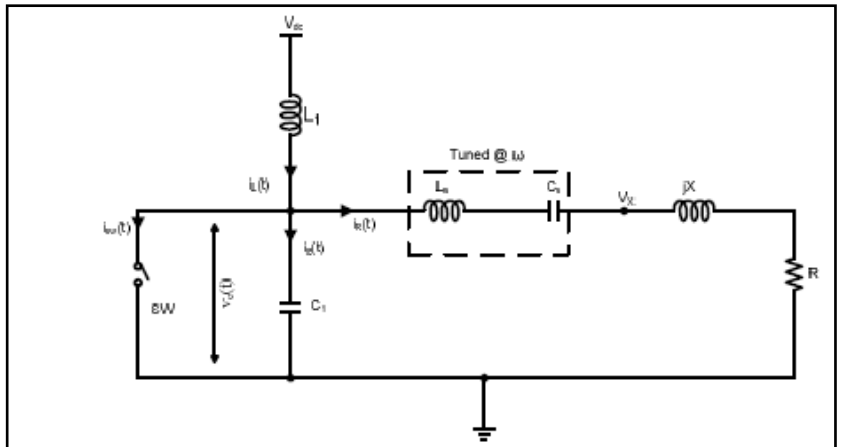
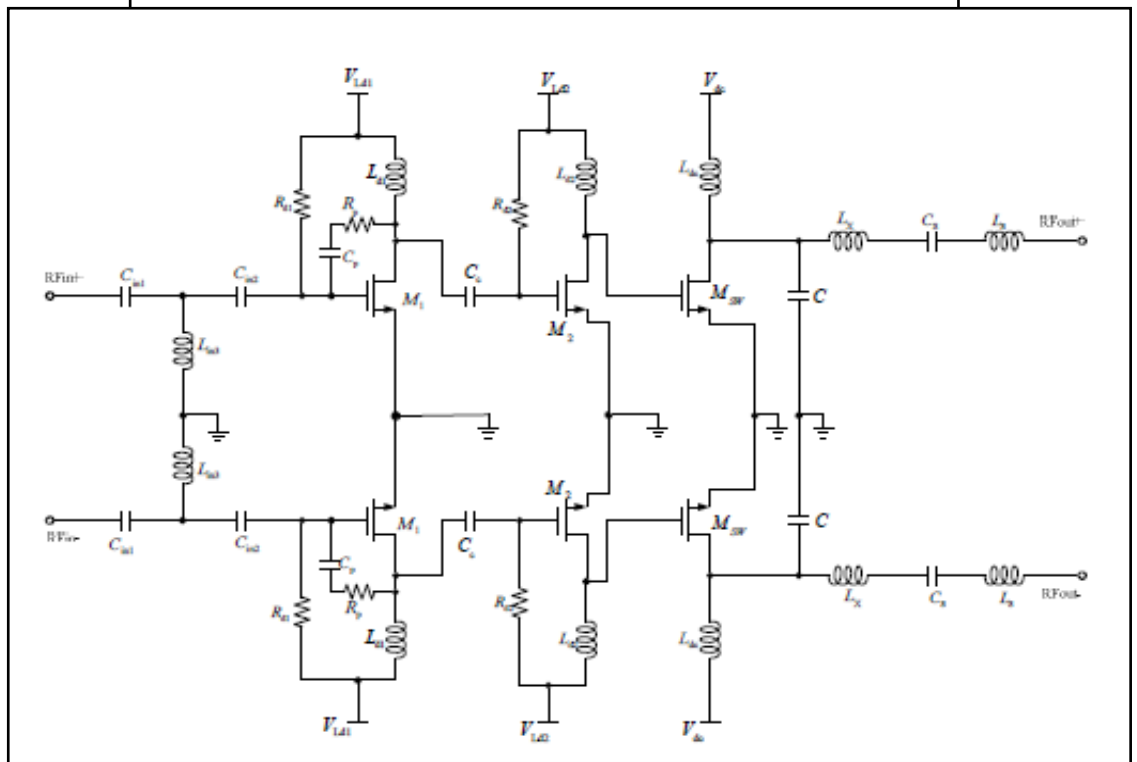


Fig. 1 The basic circuit of class-E power amplifier

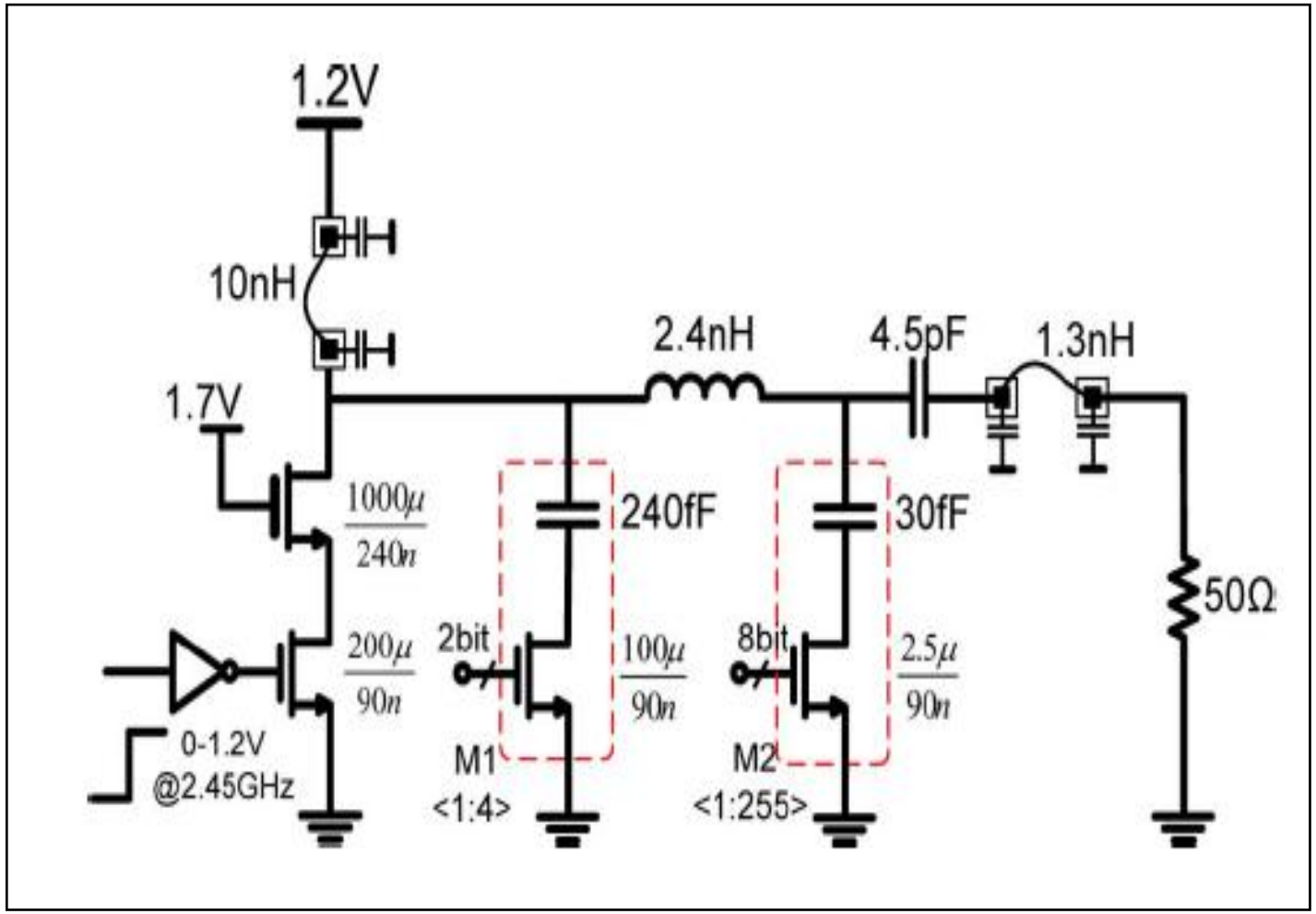


Technical Details P-1

SPECIFICATIONS	VALUE
•Technology	•TSMC 180nm
•Supply Voltage	•1V
•Saturate Output Power	•5-8dBm
•Frequency Operation	•2.4GHz
•Input power	•-10dBm
•PAE	•19%
•S11	•<-23dB
•S22	•<-9dB
•Topology	•Differential
•Year of Publication	•2013

P-2: A Digitally Modulated Class-E Polar Amplifier in 90 nm CMOS

- Class E amplifier with Digital impedance amplitude modulation.
- Suitable for moderate PAPR(Peak-to-average-power-ratio) modulation schemes (π/4 DQPSK).
- Digitally tuneable matching circuit used to perform AM and hence non-linearity is reduced.
- Peaks of both current and voltage do not overlap, minimizes power dissipation.
- Π-type network is chosen as it covers entire Smith chart.
- Net die area reduction.
- Increase in Bandwidth as phase and amplitude take different paths.
- Passive network simple in construction.

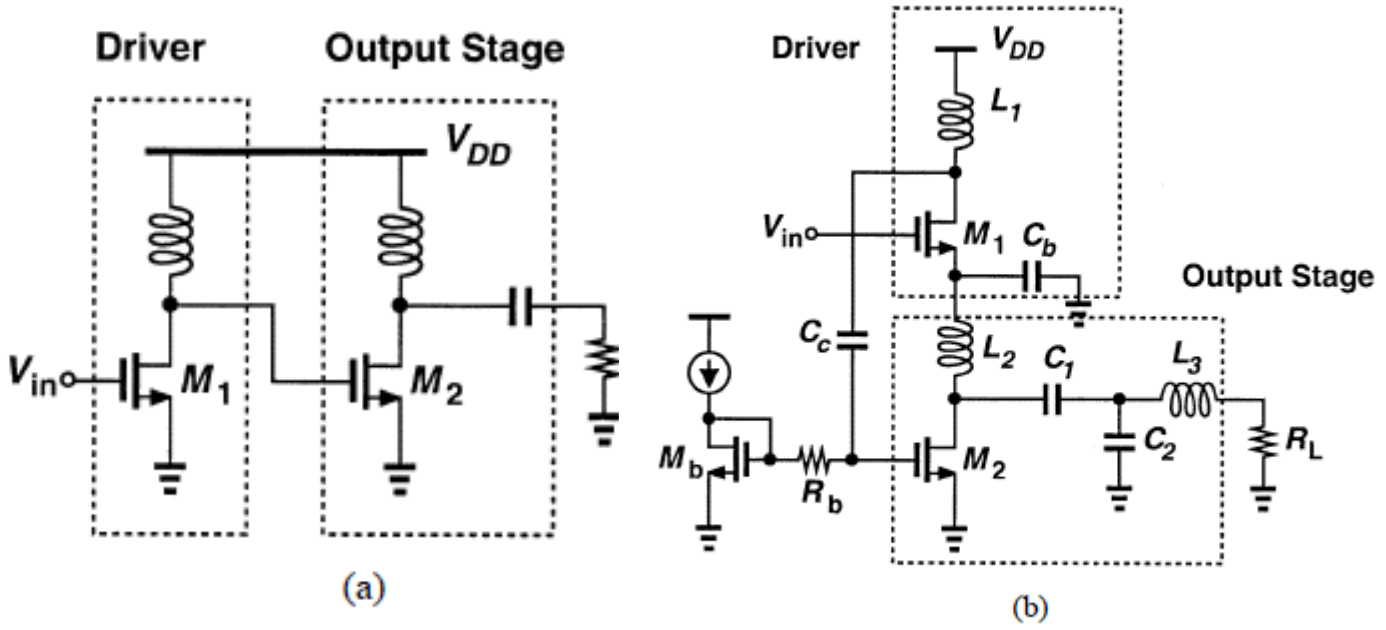


Technical Details P-2

Technology	CMOS 90nm
Supply Voltage	1.2V
Output Power	9dBm
Small Signal Gain	11dB
Frequency operation	2.4GHz
Efficiency	30%
EVM	2.6%
Die-Area	0.924 mm^2
Topology	Single Ended
Year of Publication	2012

P-3: A Low-Power 2.4GHz Transmitter/Receiver CMOS IC

- Circuit (a) suffers from high power consumption, large output swings at drain of M2, bias current must be high.
- Stacking of circuits (b) is done to mitigate drawbacks of (a).
- Advantageous as it reduces power consumption and also protects M2 from excessive drain-gate voltage.
- Dual band PA.
- Cascoding with power stage and driver to increase linearity.



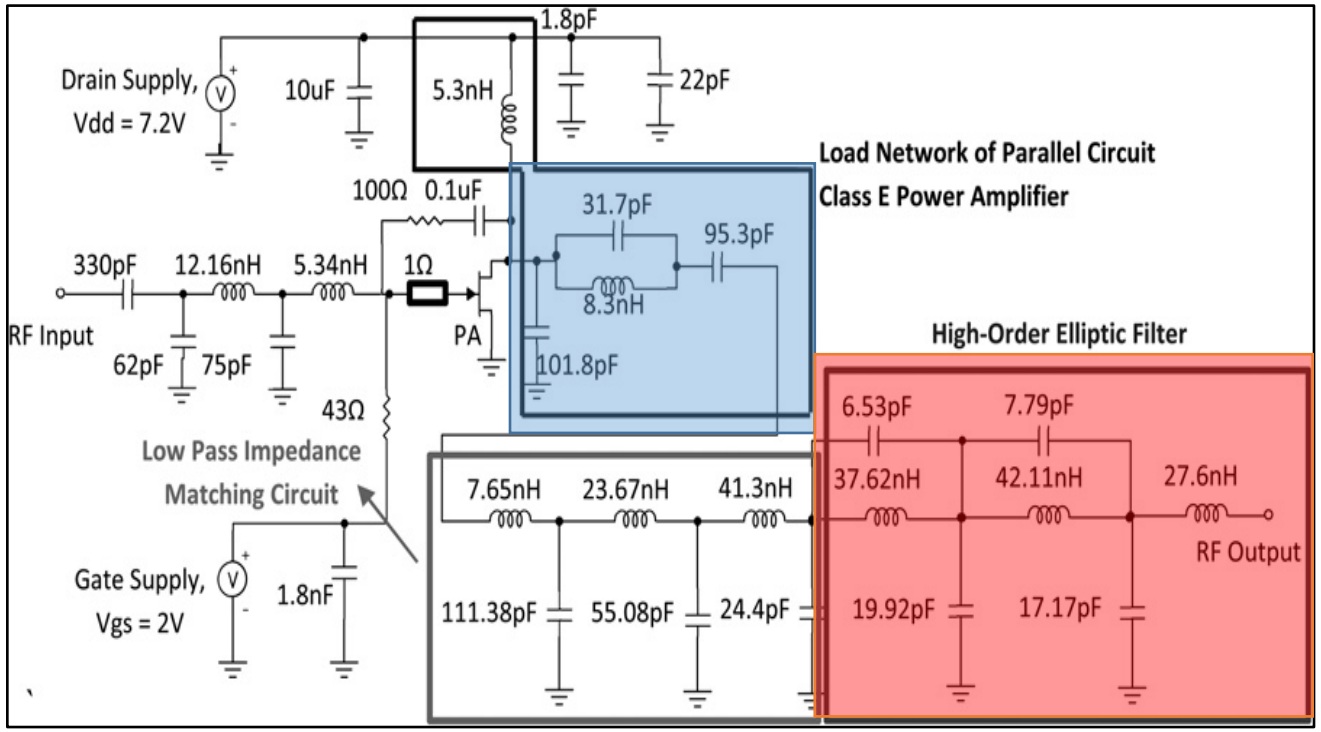
(a) Two-stage power amplifier. (b) Power amplifier circuit.

Technical Details P-3

SPECIFICATIONS	VALUE
Technology	CMOS 0.25µm
Supply Voltage	2.5V
Output Power	0dBm
Frequency Operation	2.4GHz
Output Power consumption	16mW
Bias current	3mA
Load impedance	50Ω
Die-Area	1.83mm X 2mm
Topology	Single Ended
Year of Publication	2003

P-4: Optimised high-efficiency Class E radio frequency power amplifier for wide bandwidth and high harmonics suppression

- Switch Mode Class-E PA Single ended
- Wide Bandwidth
- Combine Parallel Circuit Load
- High-Order Harmonic Suppression (single reactance compensation technique with harmonic trap at load)
- Inductive at fundamental frequencies and Capacitive at harmonic frequencies
- Combining power technique (high eff and PAE)
- Less Area and Less Cost
- Stability and Robustness has been verified



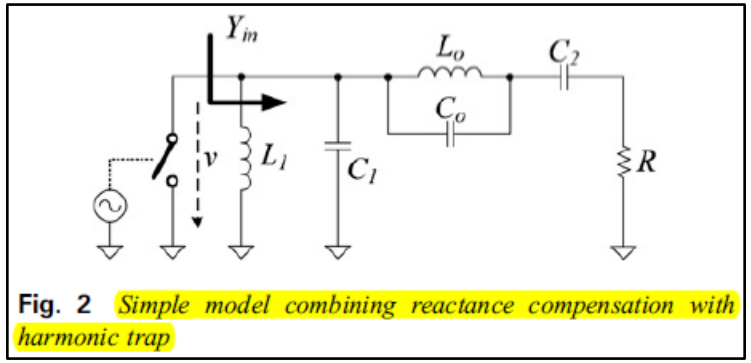


Fig. 2 *Simple model combining reactance compensation with harmonic trap*

Technical Details P-4

SPECIFICATIONS	VALUE
Technology	LDMOS
Supply Voltage	7.2V
Output Power	6.5-7W
Frequency Operation	136-174MHz
Efficiency	>60%
Second Harmonic	84dBc
Stability (10:1 VSWR)	Stable
Robustness (10:1 VSWR)	NO degradation
Drain Efficiency	71%
Topology	Single Ended
Year of Publication	2013

P-5:A 2.4 GHz 0.18-µm CMOS Class E Single-Ended Power Amplifier without Spiral Inductors

- Class-E PA Single ended.
- Bond Wire-High Q-Less area-Increased performance.
- Cascode with self-biasing to overcome device stress.
- Two Stages:
  - Driver stage (Class-A)
  - Power stage (Class-E)
- Output power changes approximately proportional to Vdd^2,
- No Baluns-reduce chip area

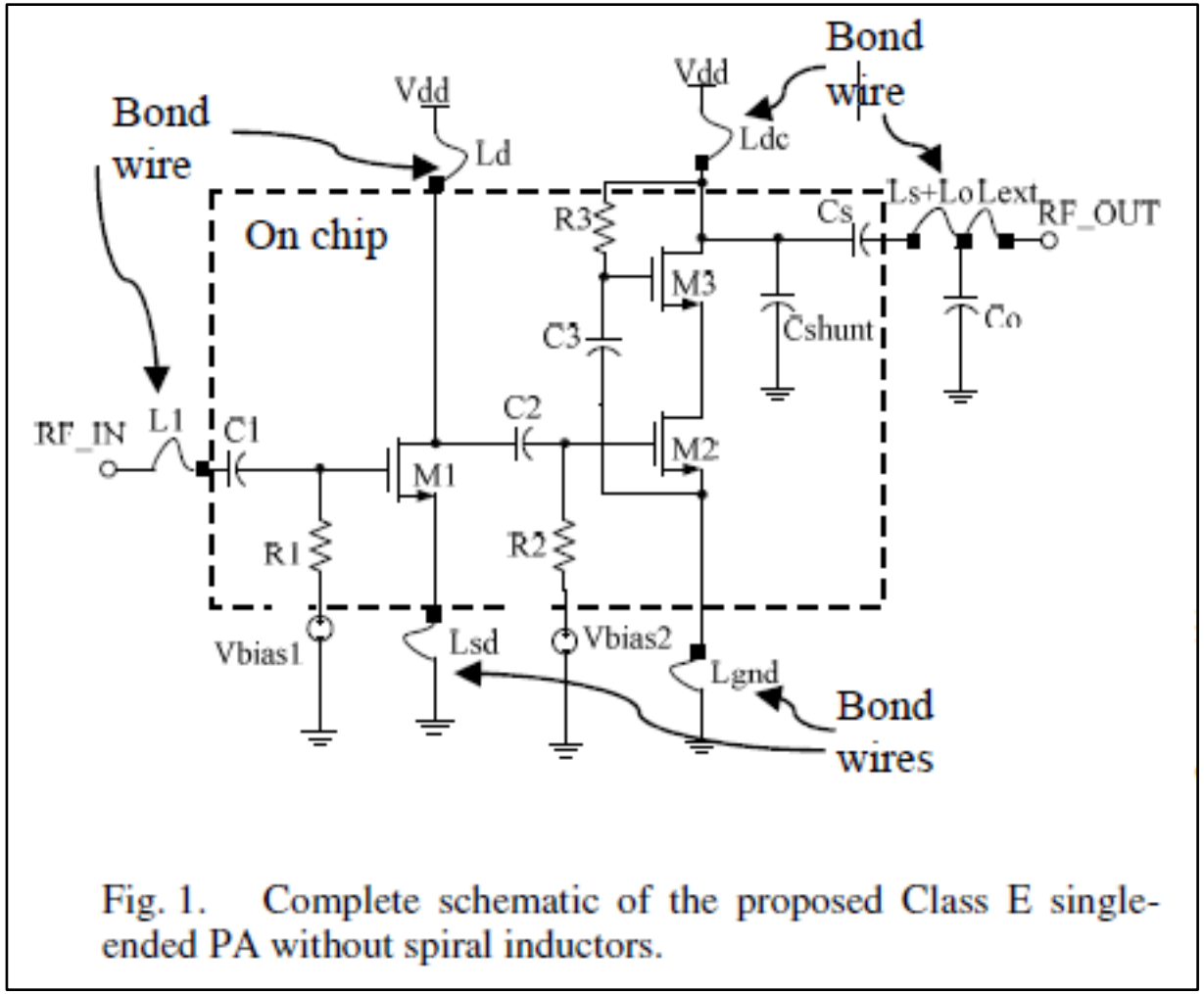


Fig. 1. Complete schematic of the proposed Class E single-ended PA without spiral inductors.

Technical Details P-5

SPECIFICATIONS	VALUE
Technology	TSMC CMOS 0.18µm
Supply Voltage	3.3V
Output Power	19.2dBm
Frequency Operation	2.35-2.45GHz
PAE	27.8%
Chip Sizes	0.37mm^2
Topology	Single-Ended
Year of Publication	2010

P-6: Design of Efficient Class-E Power Amplifiers for Short-Distance Communications

- Class-E with π-matching.
- Pre-driver and power stage to boost the power.
- PE and PAE nearly the same.

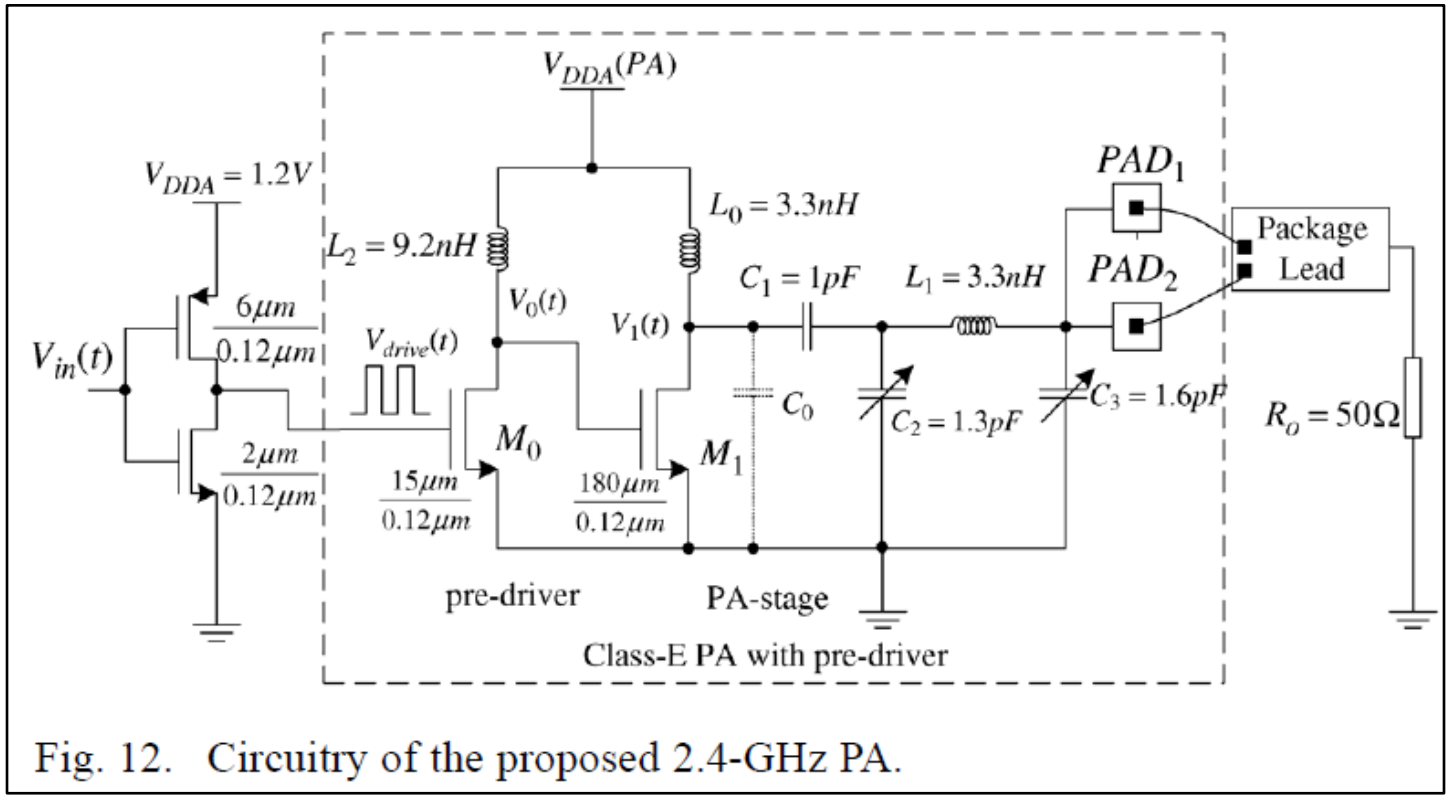


Fig. 12. Circuitry of the proposed 2.4-GHz PA.

Technical Details P-6

SPECIFICATIONS	VALUE
Technology	CMOS 0.13µm
Supply Voltage	0.45-0.8V
Output Power	3.2-5.7dBm
Frequency Operation	2.4GHz(2.2-2.5GHz)
Maximum Overall Efficiency	55%
Power Gain	20dB
Output Impedance	50Ω
Second Harmonic	-25.5dBc
Third Harmonic	-41dBc
Chip area	$0.5mm^2$
Topology	Single Ended
Year of Publication	2012

P-7: A Dual-Band CMOS Power Amplifier at 1.8 GHz and 2.6 GHz for LTE Applications

- Dual band-PA (1.8 & 2.6GHz)
- Two stage cascade structure
  - Driver stage
  - Power stage
- The driver stage uses a RC and resistive feedback-increased BW
- The power stage employs diode linearizer-linearity
- Cascade structure-low breakdown voltage-good input-output isolation-high power gain
- RC-stability of power stage-improve linearity

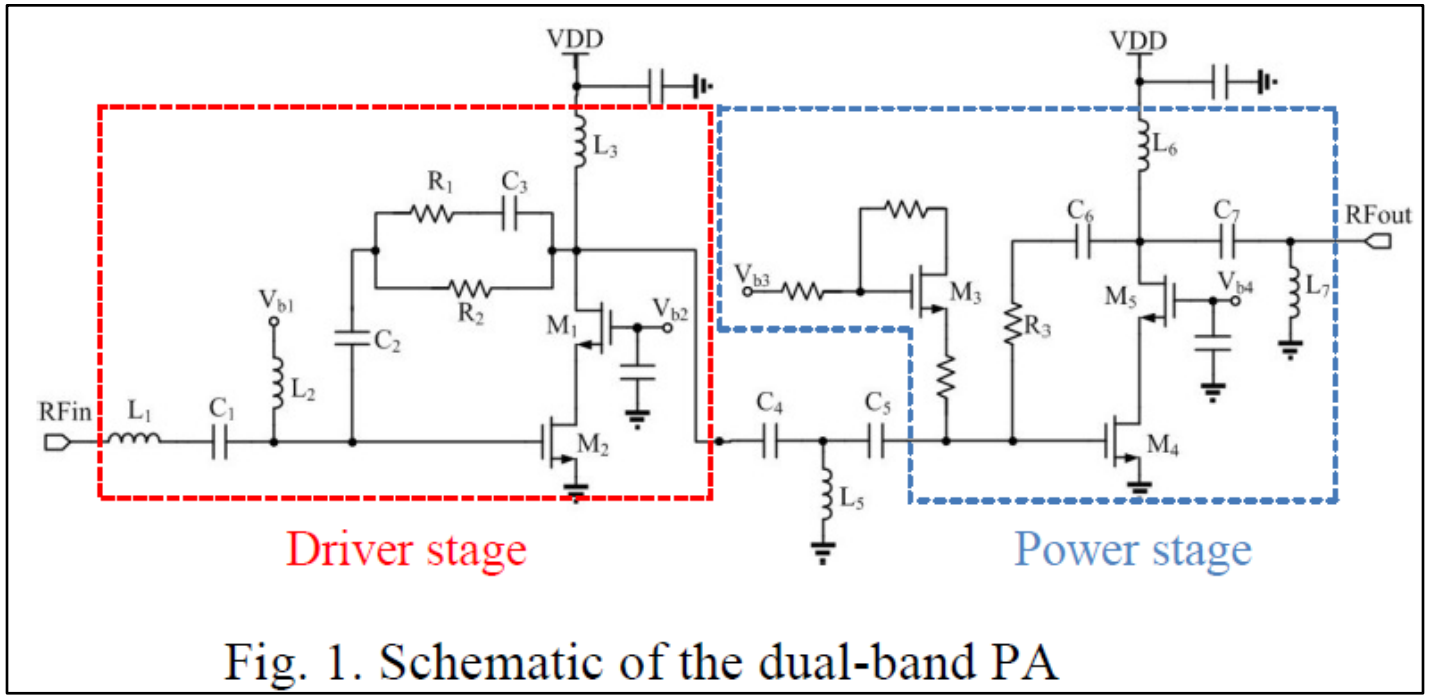


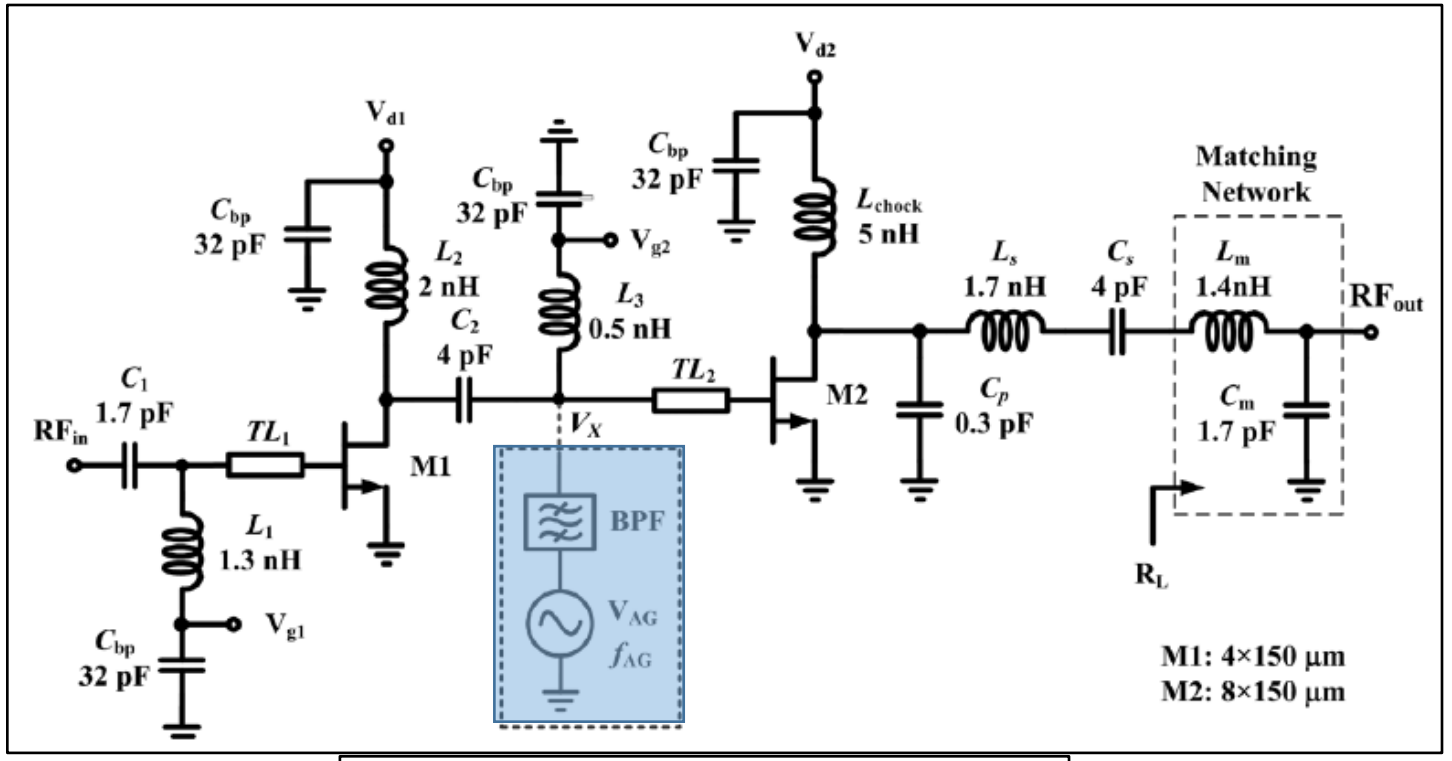
Fig. 1. Schematic of the dual-band PA

Technical Details P-7

SPECIFICATIONS	VALUE
Technology	TSMC CMOS 0.18µm
Supply Voltage	3.3V
Output Power	24.6/23.4dBm
Frequency Operation	1.8/2.6GHz
PAE	34.6/40.5%
Power Gain	22/20.2dB
Output Impedance	50Ω
Input return loss	<-18dB
Output return loss	<-8dB
Power Consumption	211mW
Topology	Single Ended
Year of Publication	2012

P-8: A Broadband Injection-Locking Class-E Power Amplifier

- Two stage Injection locking Class-E PA
- PA-oscillator-output voltage tuned to input frequency
- High PAE and Power Gain
- GMSK and 64QAM
- Two stage cascade structure
  - Driver stage
  - Power stage
- Negative resistance concept to compensate the losses
- Auxiliary generator is used for stability analysis



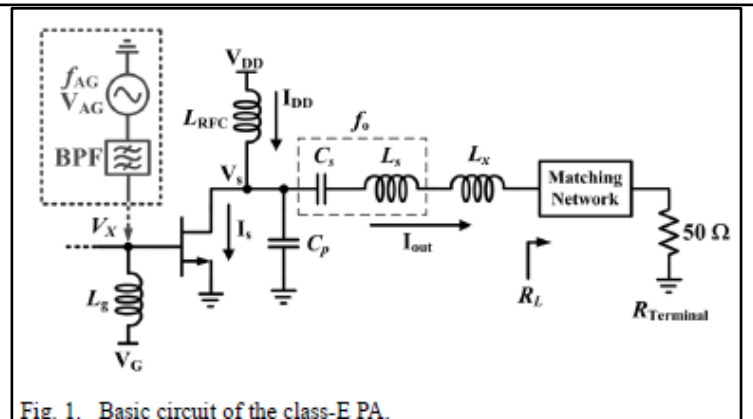


Fig. 1. Basic circuit of the class-E PA.

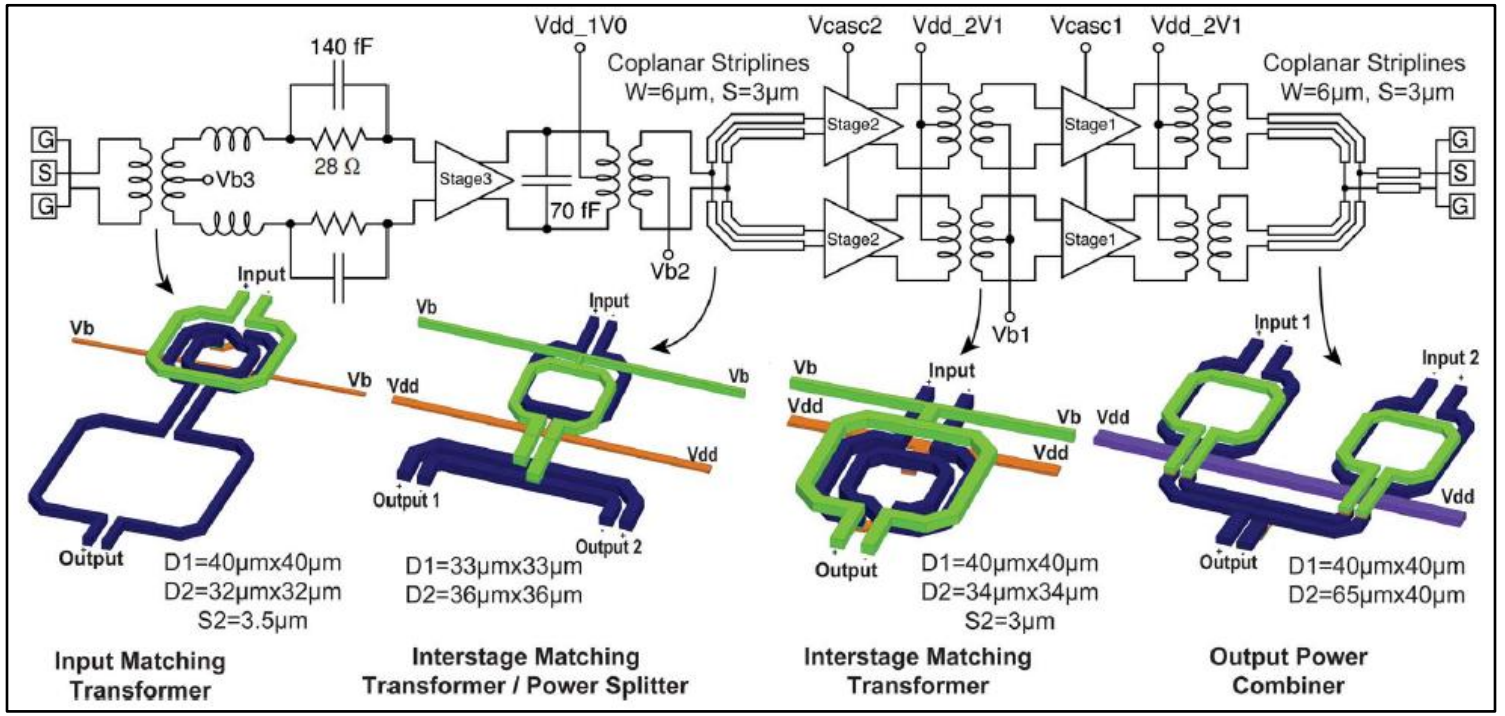
Technical Details P-8

SPECIFICATIONS	VALUE
Technology	GaAs 0.5µm
Supply Voltage	6V
Output Power	26.6/26.7/27dBm*
Frequency Operation	3.5GHz
PAE	59/57/55%*
Power Gain	30/32dB*
Drain Efficiency	58/52%*
EVM	0.75/3.08*
FOM	97.98/64.56*
ACPR-1MHz Offset	-21dBC
Topology	Single Ended
Year of Publication	2012

* Continuous wave/GMSK/64QAM

P-9: A 60 GHz Drain-Source Neutralized Wideband Linear Power Amplifier in 28 nm CMOS

- Drain-Source Neutralization-stability of PA-wideband, by low-k transformer
- Three stage cascade structure using transformers
  - Pre-Driver stage
  - Two Cascode Power stage
  - Power Combiner
- Employ DAT for higher output power
- Q-current is halved for same output power by using cascode



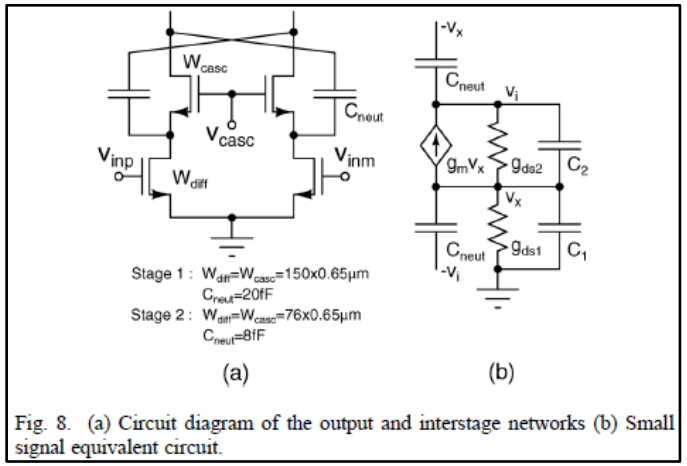


Fig. 8. (a) Circuit diagram of the output and interstage networks (b) Small signal equivalent circuit.

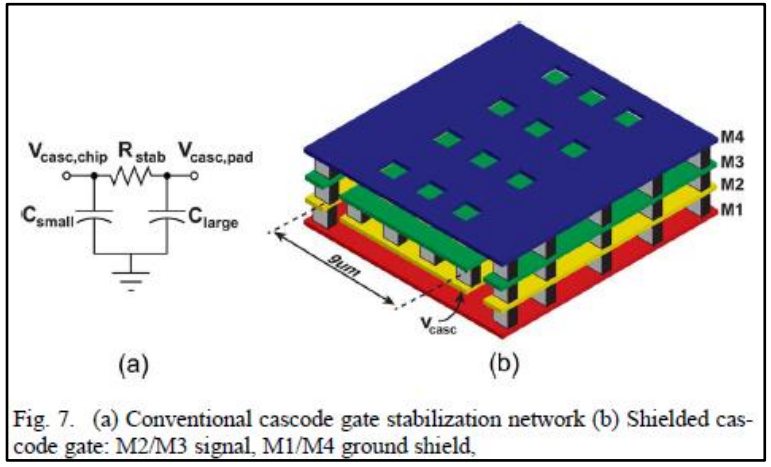


Fig. 7. (a) Conventional cascode gate stabilization network (b) Shielded cascode gate: M2/M3 signal, M1/M4 ground shield.

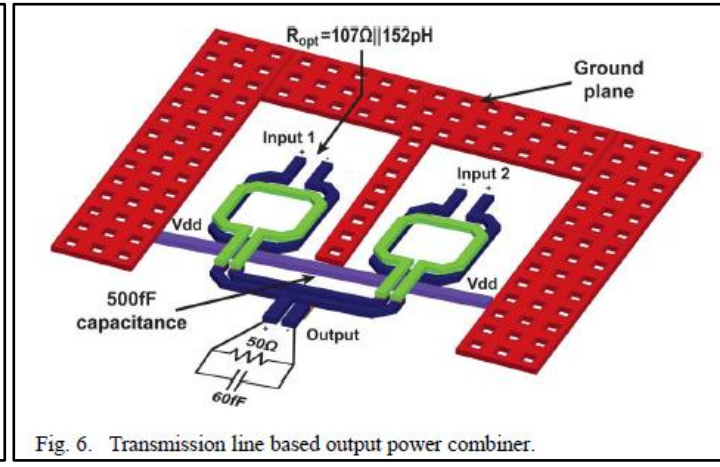


Fig. 6. Transmission line based output power combiner.

Technical Details P-9

SPECIFICATIONS	VALUE
Technology	CMOS 0.028µm
Supply Voltage	1.8-2.1V
Saturated Output Power	16.5dBm
P1-db	11.7dBm (62GHz with 6.3% PAE)
Frequency Operation	60GHz
PAE	12.6%
Power Gain	24.4dB
Bandwidth	11GHz
Power Consumption	211mW
Chip Area(core/total)	0.122/0.64mm^2
Topology	Differential
Year of Publication	2014

P-10: A Fully Integrated Transformer-Coupled Power Detector With 5 GHz RF PA for WLAN 802.11ac in 40 nm CMOS

- WLAN 802.ac
- Single stage PA with transformer I/O matching
- Consists of common gate and common source topology
- CG allows increasing power supply which allows achieving higher output power while operating reliably

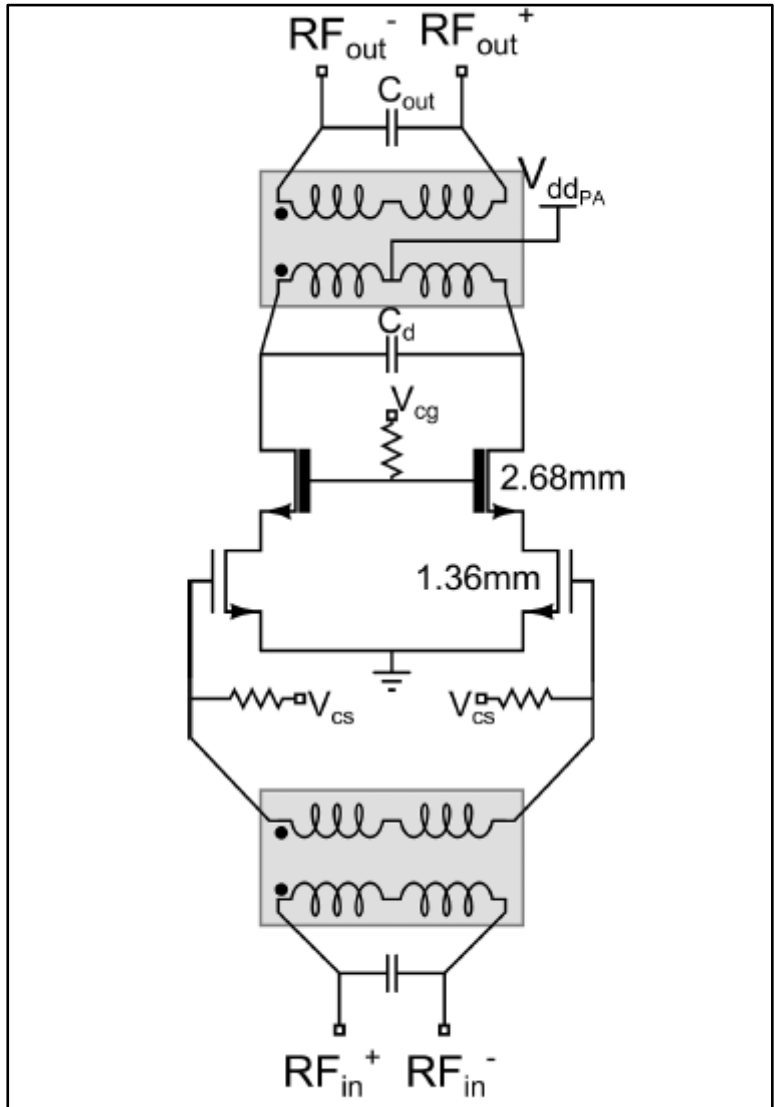


Fig. 9. Simplified schematic of the 5 GHz RF PA for WLAN IEEE 802.ac.

Technical Details P-10

SPECIFICATIONS	VALUE
Technology	TSMC CMOS 0.040µm
Supply Voltage	2.5V
Saturated Output Power	22.9dBm
Output Power	24dBm
Frequency Operation	4.5-5.5GHz
PAE	38.8%
Power Gain	10dB
Output Impedance	50Ω
Peak Drain Efficiency	40.8%
Topology	Differential
Year of Publication	2015

P-11: A CMOS High Efficiency +22 dBm Linear Power Amplifier

- Parallel A&B PA
- Improves dynamic range and power efficiency
- Increase P1dB by 3dB and reduces power consumption by 50% in the linear operation range
- Class A amplifier is the primary contributor for gain at the low signal levels, however class B at the high signal levels.
- Shunt inductors L_{in} are used to match the inputs, and the inductors RFC are used as RF chokes to prevent coupling of the RF signal to the power supplies and inductors L_o is used to match the output port.

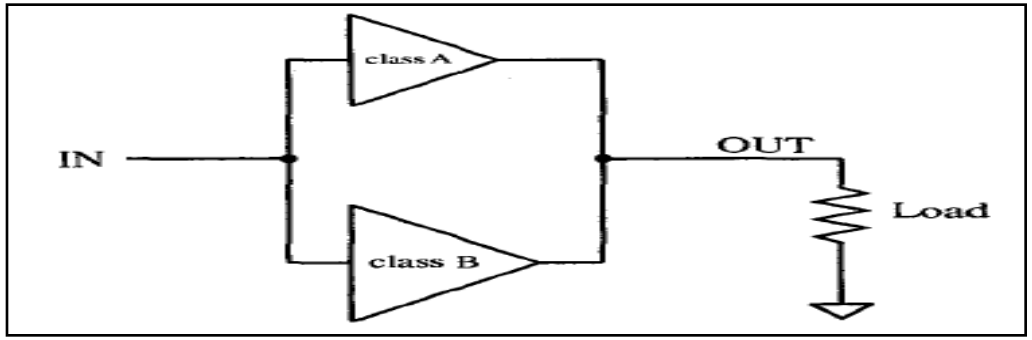
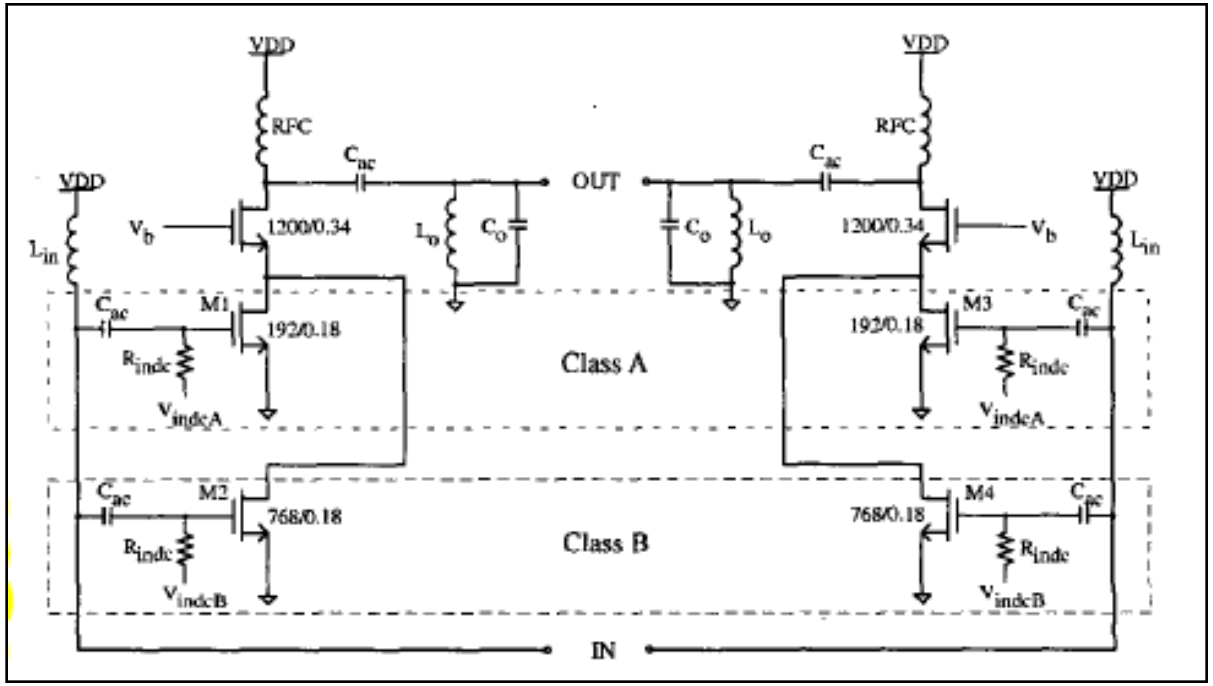


Fig:-Conceptual block diagram of parallel A&B amplifier



Technical Details P-11

SPECIFICATIONS	VALUE
Technology	CMOS
Output Power	22dBm
PAE	>40%
Linear Power Gain	12dB
P1dB	20.5dBm
Year of Publication	2003

P-12: Design of CMOS Class-E Power Amplifier for WLAN and Bluetooth Applications

- Class-E PA with modified driver
- Better output power at minimum input power levels
- Negative capacitance to reduce parasitic capacitance without external circuitry
- Better power gain at cost of extra hardware

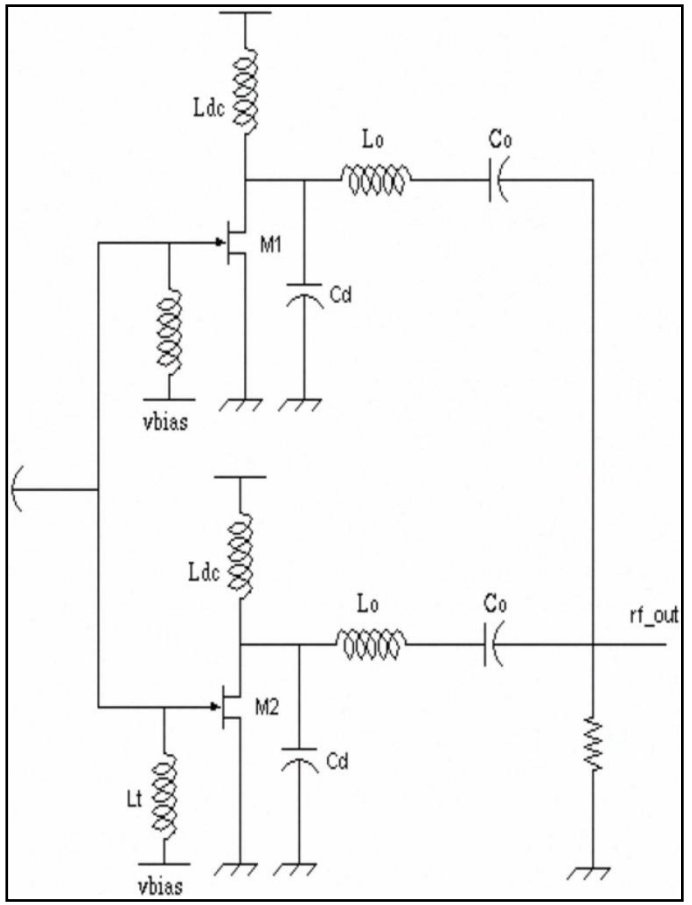


Fig:-Parallel PA

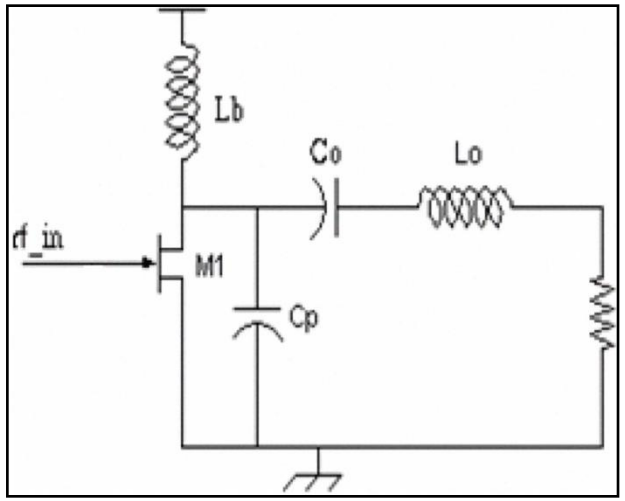


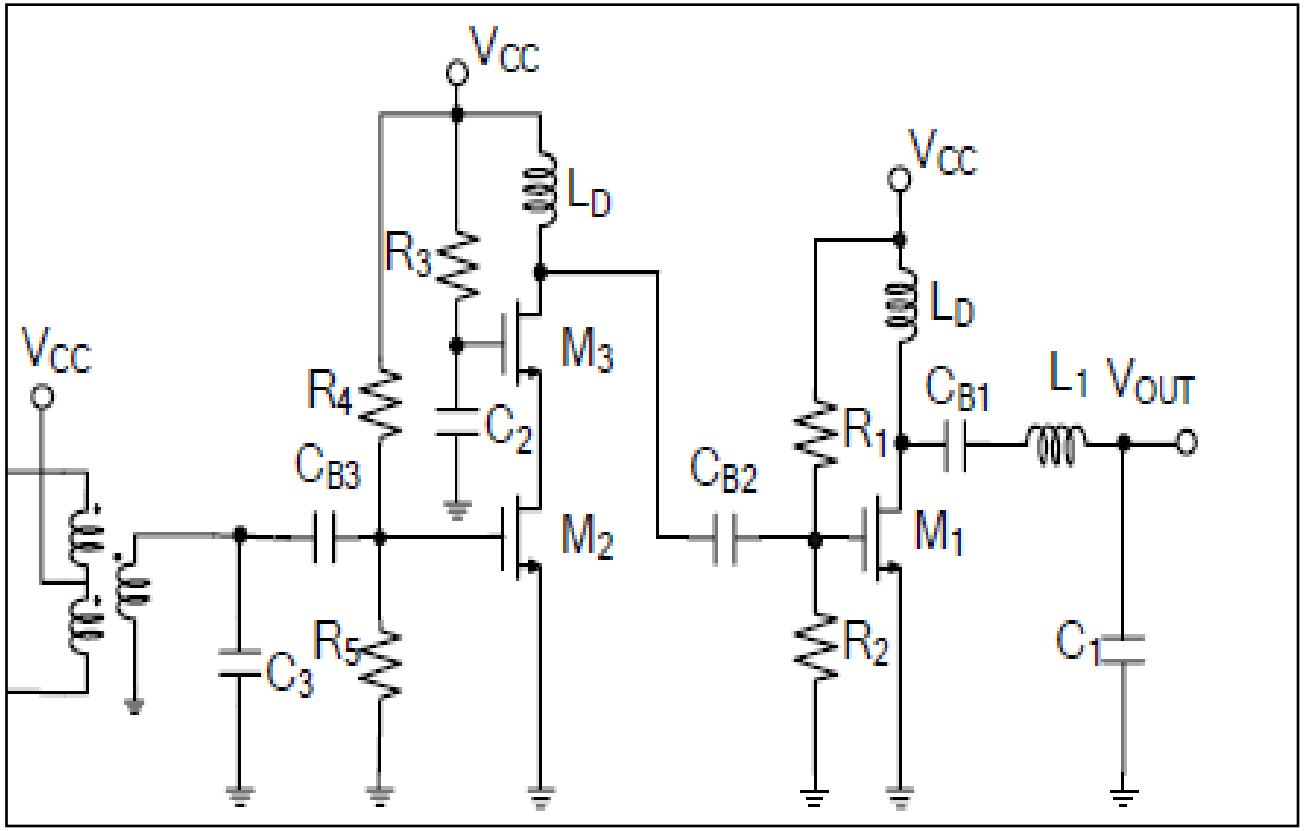
Fig:- single ended class E PA

Technical Details P-12

SPECIFICATIONS	VALUE
Technology	UMC CMOS
Supply Voltage	1.8V
Gain	20dBm
Frequency Operation	2.4GHz
PAE	40%
Topology	Single ended
Year of Publication	2012

P-13: Low-Power RF Transceiver for IEEE 802.15.4 (ZigBee) Standard Applications

- Two stage PA
- Low power
- Consists of class A pre-amplifier that drives the high efficient class C amplifier.
- Class C amplifier has been designed with conduction angle of 150 degrees, which allowed to achieve good tradeoff between efficiency and gain.
- The PA can provide an output power up to of 6 dBm when it is driven with an input power of -15 dBm supplied by the class-A driver stage.



Technical Details P-13

SPECIFICATIONS	VALUE
Technology	BiCMOS
Supply Voltage	1.8V
Output Power	6dBm
Saturated output power	8dBm
Power Consumption	16mW
Topology	Single Ended
Year of Publication	2006

P-14: A Highly Linear and Efficient CMOS RF Power Amplifier With a 2-D Circuit Synthesis Technique

- Class A tanh cascode cell(TCC) amplifier
- Linearization with 2DCST over wide range
- Doesn't require inverse circuit for amplitude correction
- TCC is used to realize class AB amplifier having tanh-like current voltage characteristic
- The total current is the linear sum of cell currents
- Linearity can be synthesized by appropriate sizing and scaling of the current-voltage transfer characteristic of individual cell

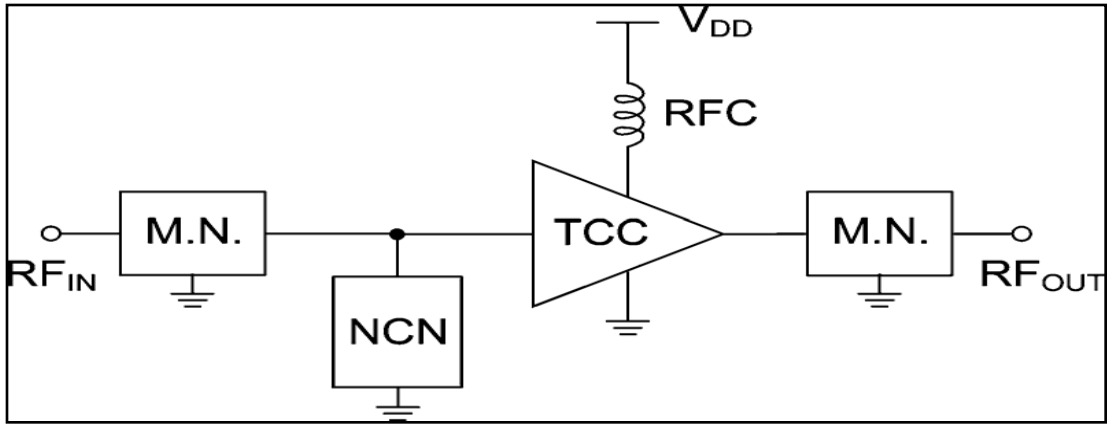


Fig:-TCC CMOS RF PA

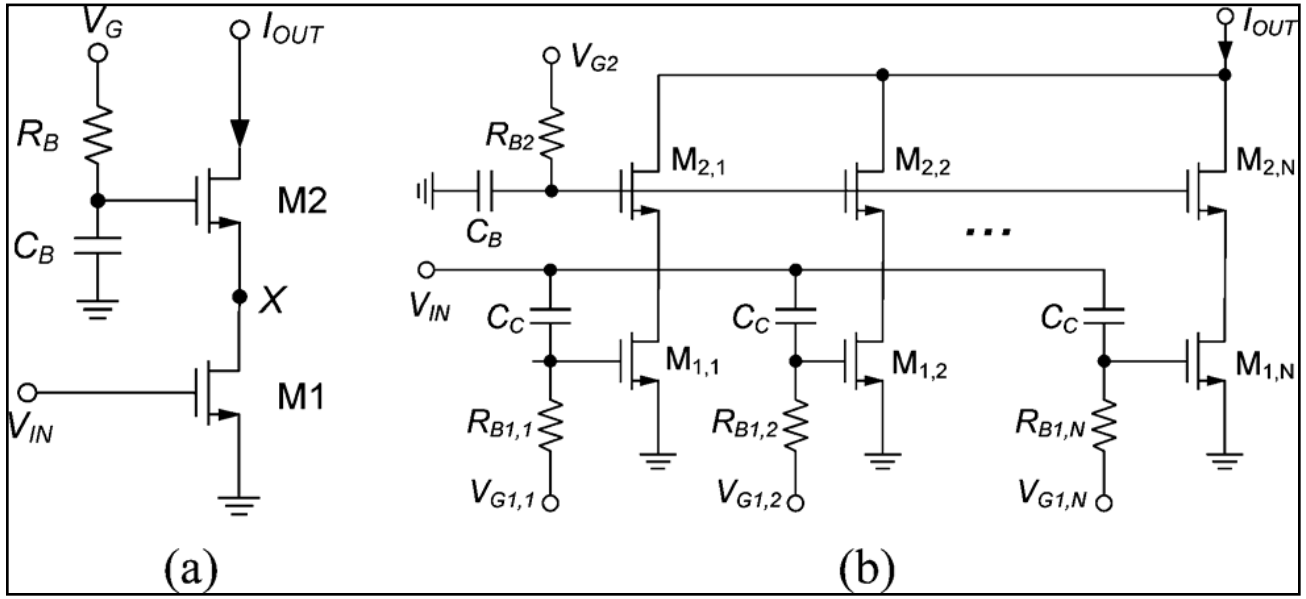


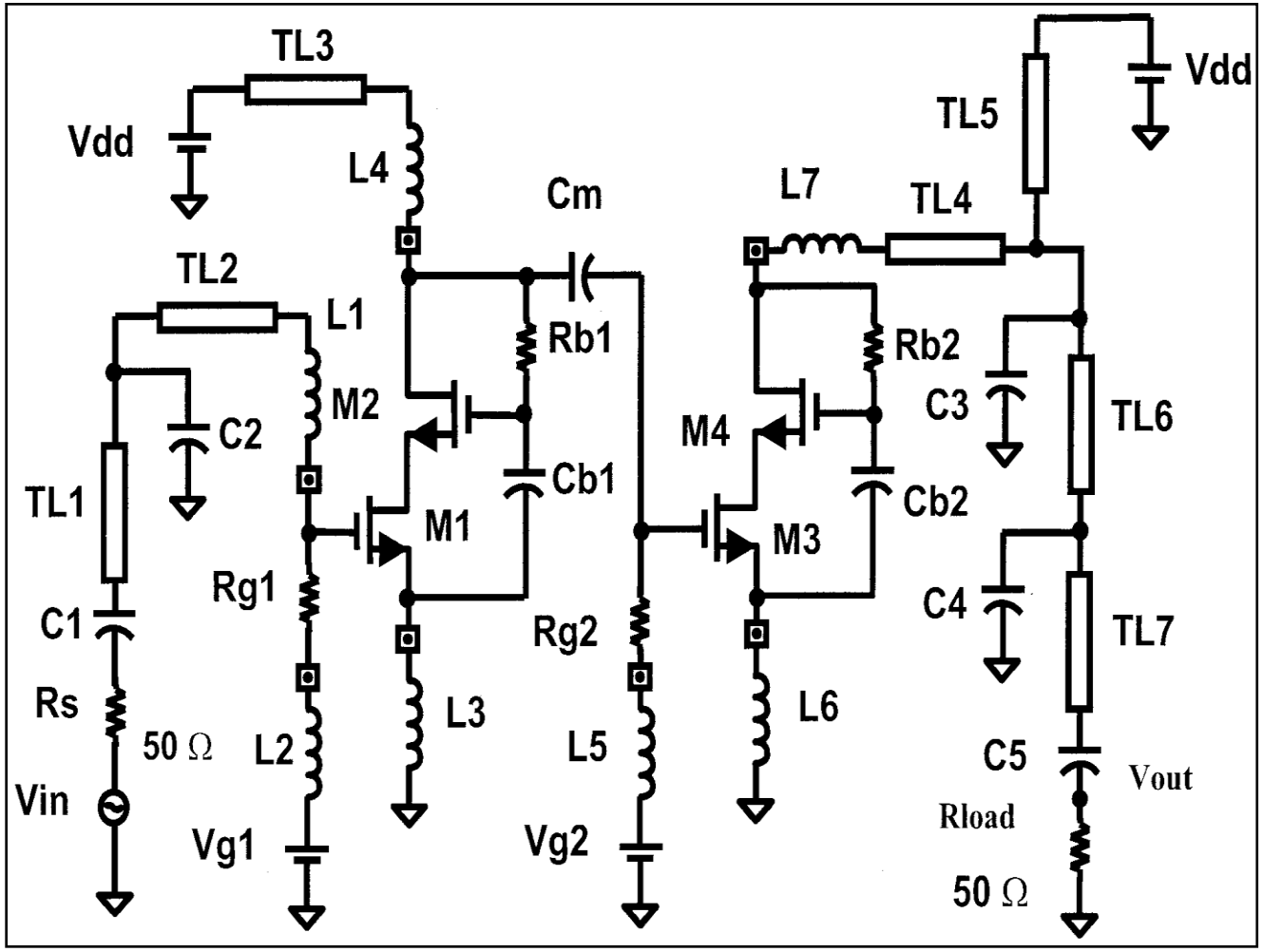
Fig:- TCC amplifier

Technical Details P-14

SPECIFICATIONS	VALUE
Technology	CMOS
Output Power	24.9dBm
Efficiency	41.6%
Topology	Single Ended
Year of Publication	2012

P-15: A 2.4-GHz 0.18-um CMOS Self-Biased Cascode Power Amplifier

- Two stage self biased cascode PA
- Equivalent total gain is of three stages
- Self biased cascoding reduces maximum drain-gate voltage across each transistor.
- Input and Output matching are designed to be off- chip to increase matching flexibility and avoid excessive power loss of on- chip inductors
- Traces on the PCB are used as transmission lines as a part of input, inter-stage and output matching networks(TL1-TL7)
- A two step matching network is used to transform load to optimum load, composed of TL4-TL7 and parallel capacitors C3 & C4 , which short circuit the second and third harmonics to ground



Technical Details P-15

SPECIFICATIONS	VALUE
Technology	CMOS
Supply Voltage	2.4V
Output Power	23dBm
Frequency Operation	2.4GHZ
Efficiency	42%
Small Signal Gain	38dBm
Large Signal Gain	31dBm
Area	0.81mm x 0.57mm
Topology	Single Ended
Year of Publication	2003