Low Noise Amplifier

Literature Survey

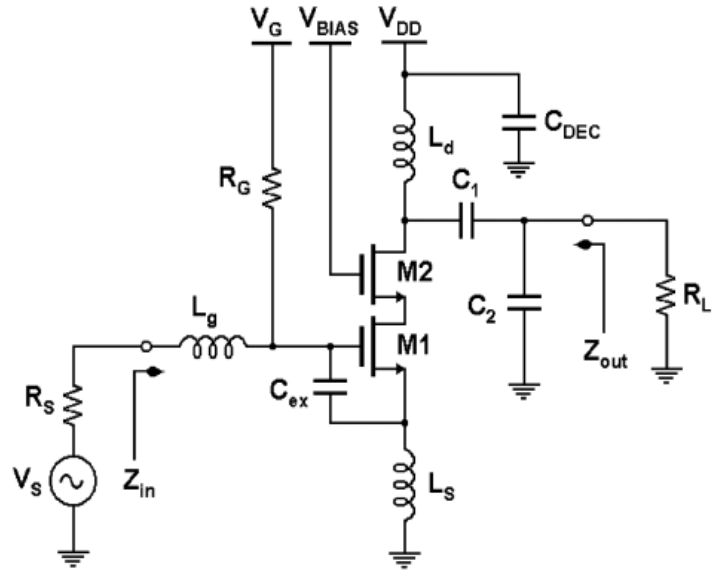
SUCHITAV KHADANGA

RFIC TECHNOLOGIES, BANGALORE, INDIA

http://www.rficdesign.com

Paper-1:

A 2.4-GHz Fully Integrated ESD-Protected Low-Noise Amplifier in 130-nm PD SOI CMOS Technology

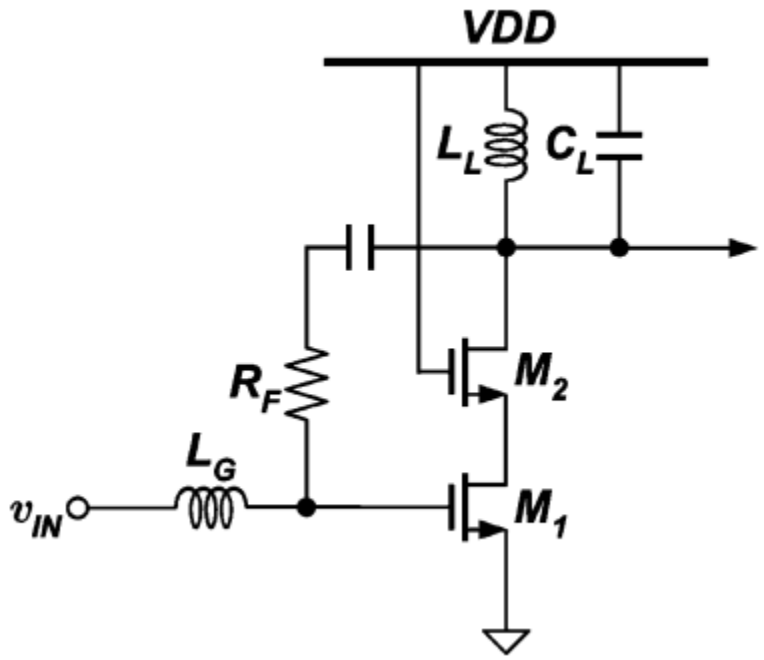


Year of publication	2007
Technology	130 nm SOI
Noise Figure	3.6 dB
Supply Voltage	1.2 V
Gain	13 dB
S_{11}	-14 dB
S_{22}	-12 dB
S_{12}	-19 dB

- Capacitor in parallel to C_{gs} is employed in this design.
- From $f_0 = \frac{1}{2\pi\sqrt{(L_g + L_s)(C_{gs} + C_{ex})}}$

Increase in the C_{ex} allows in the usage of an on chip inductor.

Paper-2:
A 2.4-GHz Resistive Feedback LNA in 130 nm CMOS

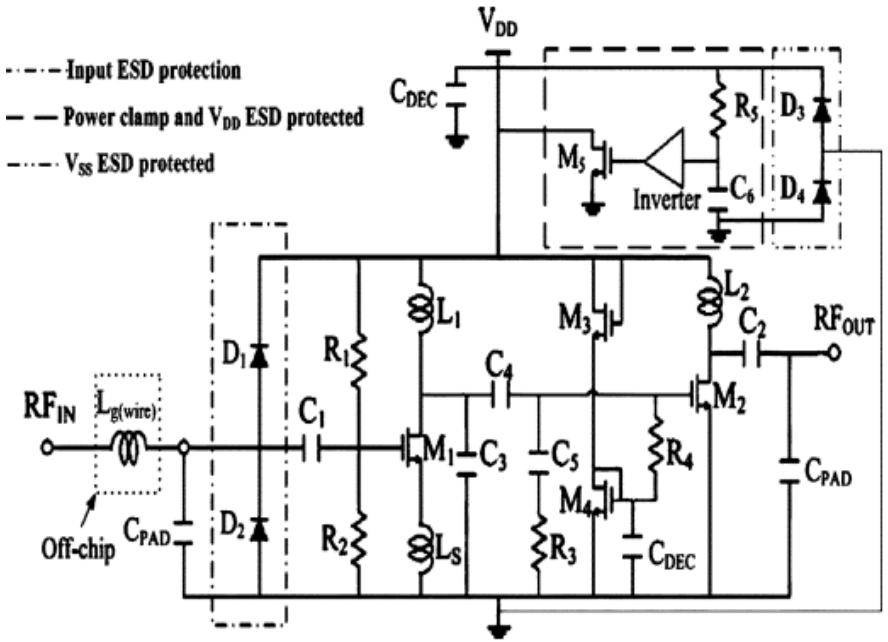


Year of publication	2009
Technology	130 nm CMOS
Noise Figure	2 dB
Supply Voltage	1.2V
Gain	24 dB
S_{11}	-10.7 dB
S_{22}	-7.6 dB

- Adopts the advantages of both L-CSLNA (Common source with inductive degeneration LNA) and RFLNA(Resistive feedback LNA)
- NF of 1.2 dB can be gained if external matching is used.
- The resistive feedback results in increase of g_m. This results in increased gain.
- It reduces the L_g required as effective capacitance at gate-source junction increases, making it realisable on-chip.
- This also results in an increase in the degrees of freedom in the input matching.

Paper-3 :

A High Gain and Low Supply Voltage LNA for the Direct Conversion Application With 4-KV HBM ESD Protection in 90-nm RF CMOS

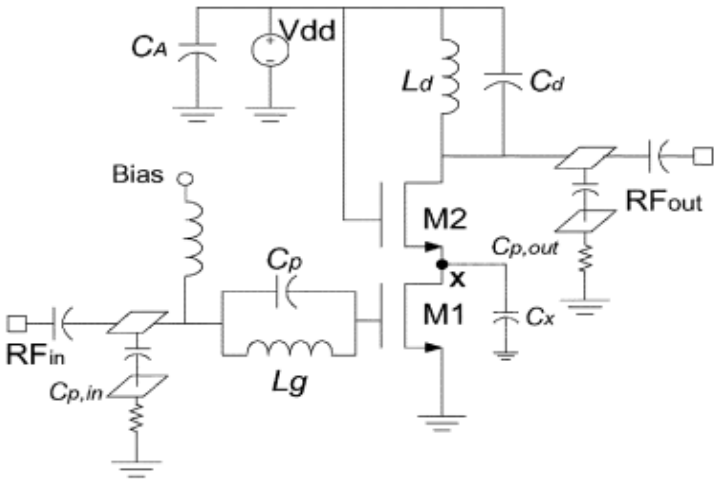


Year of publication	2006
Technology	90 nm CMOS
Noise Figure	3.2 dB (with ESD), 2.56 dB (w/o)
Supply Voltage	1 V
Gain	22 dB
S_{11}	-11 dB(w), -12.66 dB (w/o)
S_{22}	-18.35 dB(w), -19.45 dB (w/o)

- L_g used here is external.
- This is a cascaded structure with M_1 and M_2 acting as the two stage amplifiers.
- C_1 is used as the DC blocking capacitance.
- L_1 , C_3 , C_5 , R_3 are used for inter-stage matching.
- M_3 and M_4 acting as current mirrors provide the DC biasing for M_2 . R_1 and R_2 provide the resistive DC biasing for M_1 .
- The dotted box indicates the protection circuitry for the design.

Paper-4:

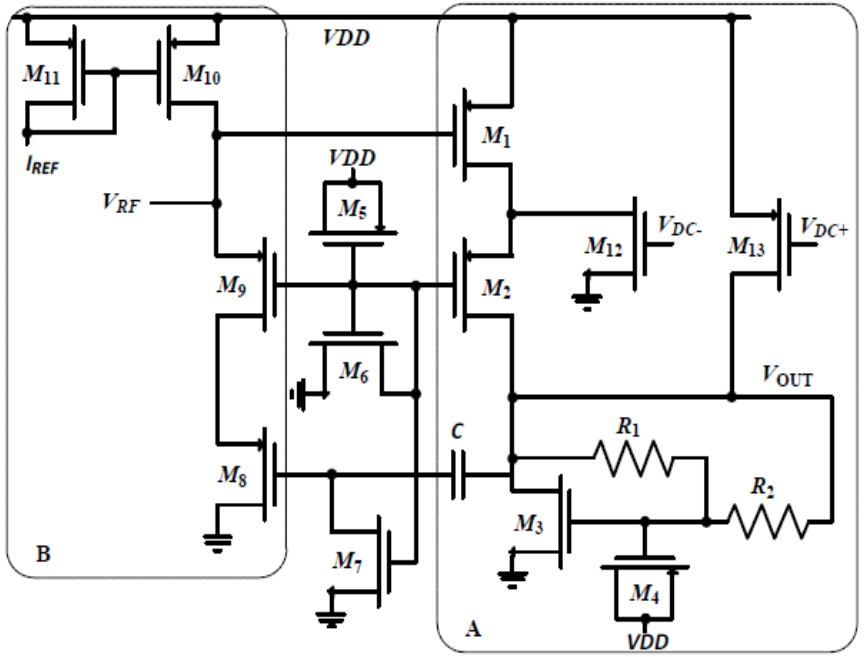
A Modified Architecture Used for Input Matching in CMOS Low-Noise Amplifiers



Year of publication	2005
Technology	180 nm CMOS
Noise Figure	2.62 dB to 2.8 dB
Supply Voltage	1.5 V
Gain	24 to 25 dB
S_{11}	-18.5 dB to -14.4 dB
S_{22}	-12 dB to -11dB
S_{12}	-31 dB to -27.5 dB

- Inductance at input is increased by placing a capacitor in parallel to L_g.
- $L_{eff} = \frac{L_g}{1-(\frac{w}{w_{o1}})^2}$
- Parasitic resistance of the used inductor also helps in appropriate input matching.
- Thus, L_s can be reduced or removed.

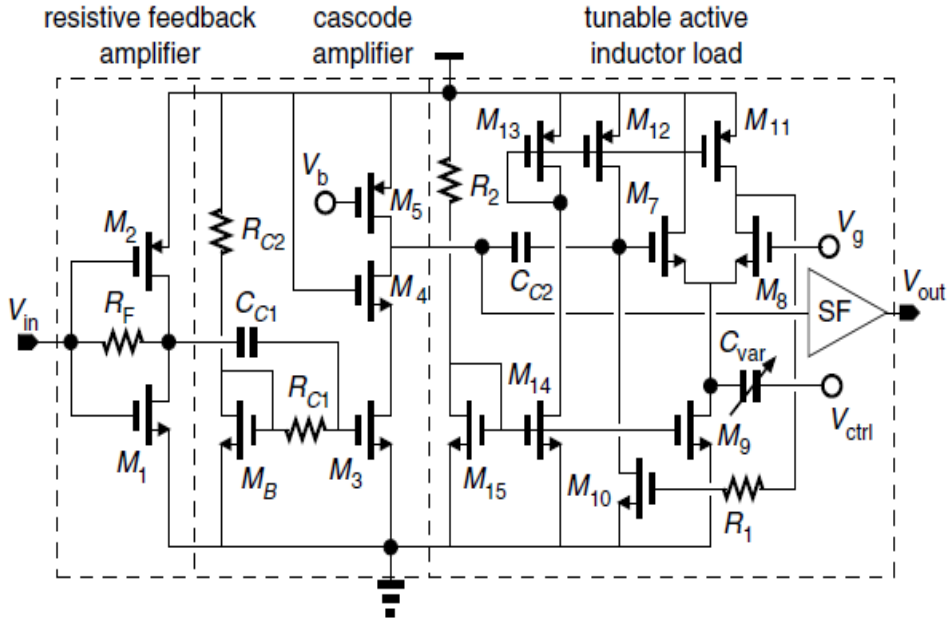
Paper-5 :
A 2.41 GHz ISM Receiver using an IQ VCO-Mixer



Year of publication	2015
Technology	130 nm CMOS
Noise Figure	3.16 dB (feedback LNA only)
Supply Voltage	1.2 V
Gain	16.8 dB
S_{11}	-15.4 dB

- Inductor less RF CMOS front end solution is one of the main advantages of this paper.
- Feedback LNA is used in this design, with common source as amplifying stage(M_1 and M_2).
- Feedback stage is a common drain design (M_8 and M_9).
- M_7 , M_2 and M_9 are biased by M_6 .

Paper-6:
Compact inductor less CMOS low-noise amplifier for reconfigurable radio



Year of publication	2014
Technology	130 nm CMOS
Noise Figure	< 3.5 dB
Supply Voltage	2. V
Gain	> 20 dB
S_{11}	< -12 dB
S_{22}	< -14dB
Frequency range	1.8 GHz to 2.4 GHz
Active silicon area	0.052 mm^2

- Cascode amplifier with a tuneable active LC resonator is added for high gain and continuous tuning of bands.
- Consists of resistive current reuse feedback amplifier and Cascode amplifier.
- LNA is realised using less active silicon area.