

Aim: To design an inverter, nand & nor and perform the following operations

- 1) Schematic simulation
- 2) Calculation of rise time, fall time, delay, power consumption.
- 3) Creation of layout and performing DRC, LVS and RCX.
- 4) Performing post layout simulation

Procedure:

- A schematic was done for the inverter and its functionality was verified.

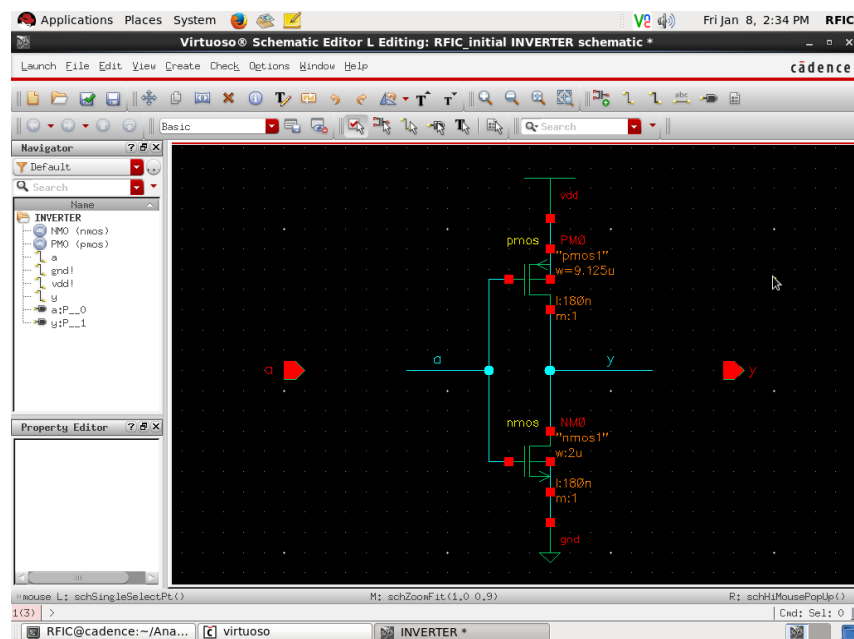


Figure 1 Schematic of Inverter

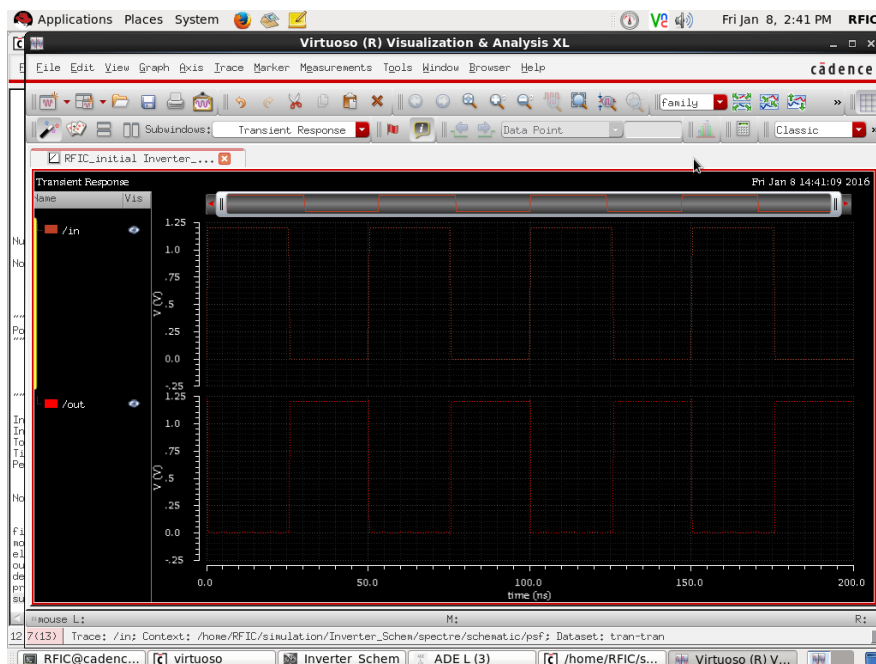


Figure 2 Functional verification of Inverter

- Sizing was done so that the switching threshold was half of V_{dd} and it was made sure that rise and fall times of the outputs are nearly equal. W_n was decided to be $2u$ and W_p as $9.125u$.
- Output rise and fall times were calculated to be $101p\ s$ and $95p\ s$ respectively, when input rise and fall times were both kept at $500p\ s$. These were done using the rise and fall time functions in the calculator.

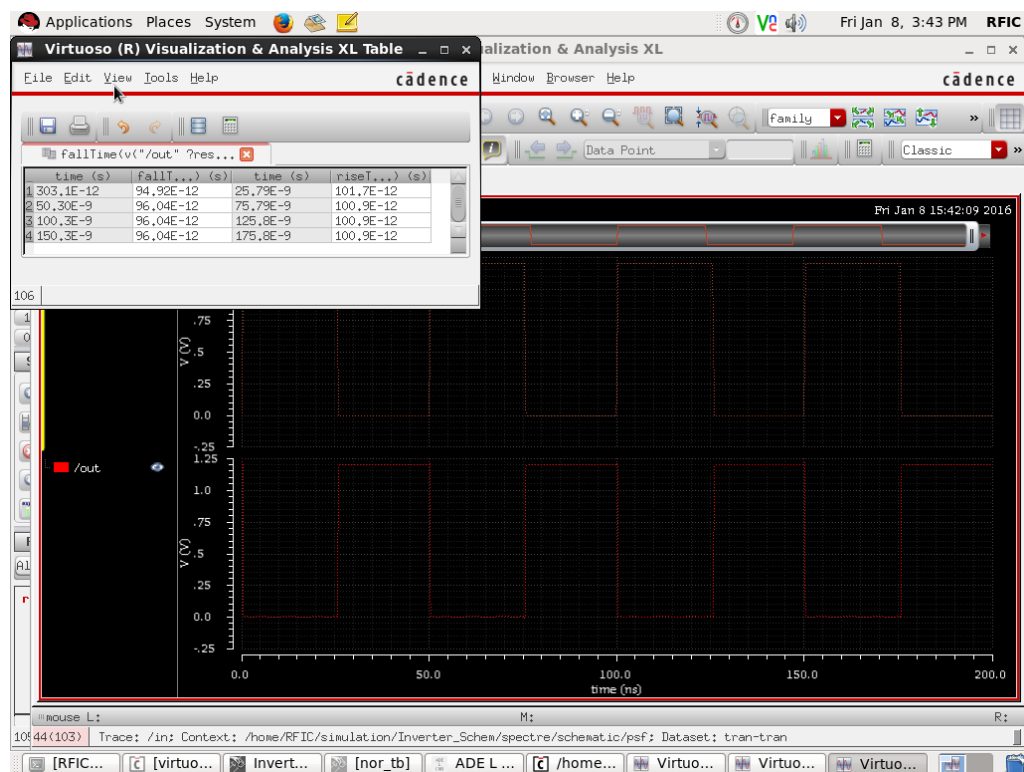


Figure 3 Calculation of rise time and fall time of the Inverter

- Average power consumption was calculated as $576.7n\ W$. Static power dissipation was found by making sure that there was no switching activity in the circuit and it was found to be $14.11p\ W$.

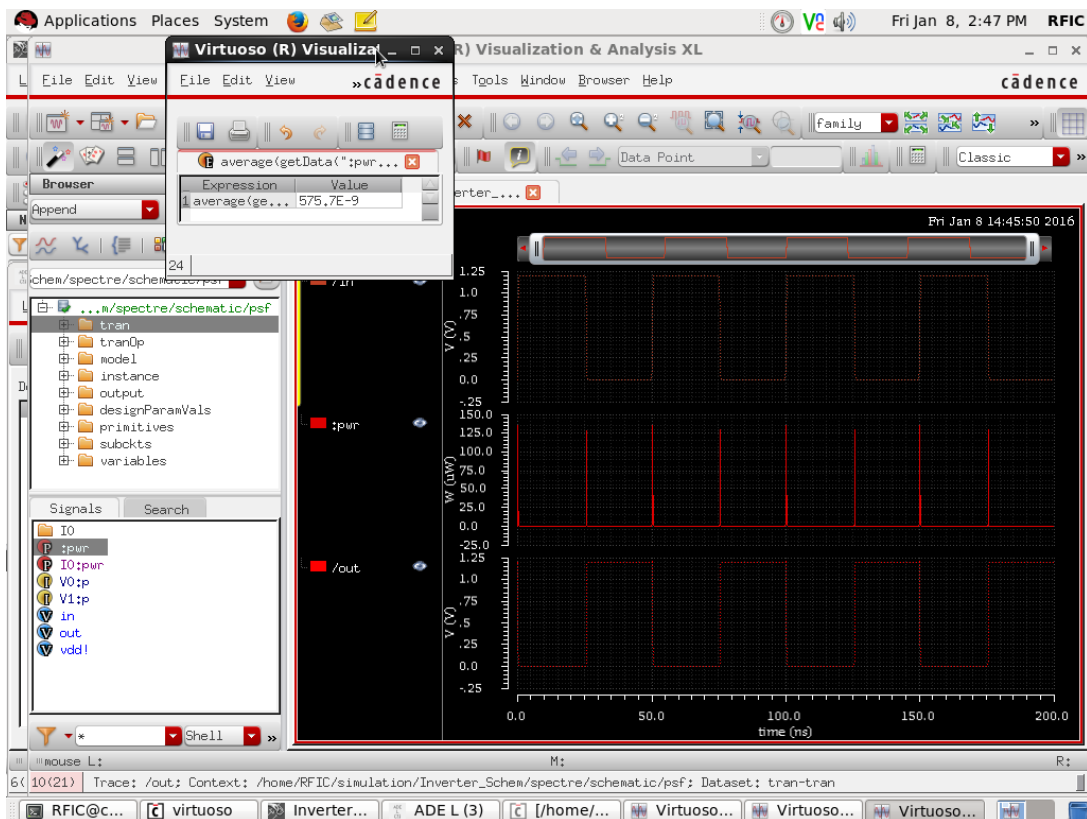


Figure 4 Total power consumption of the Inverter

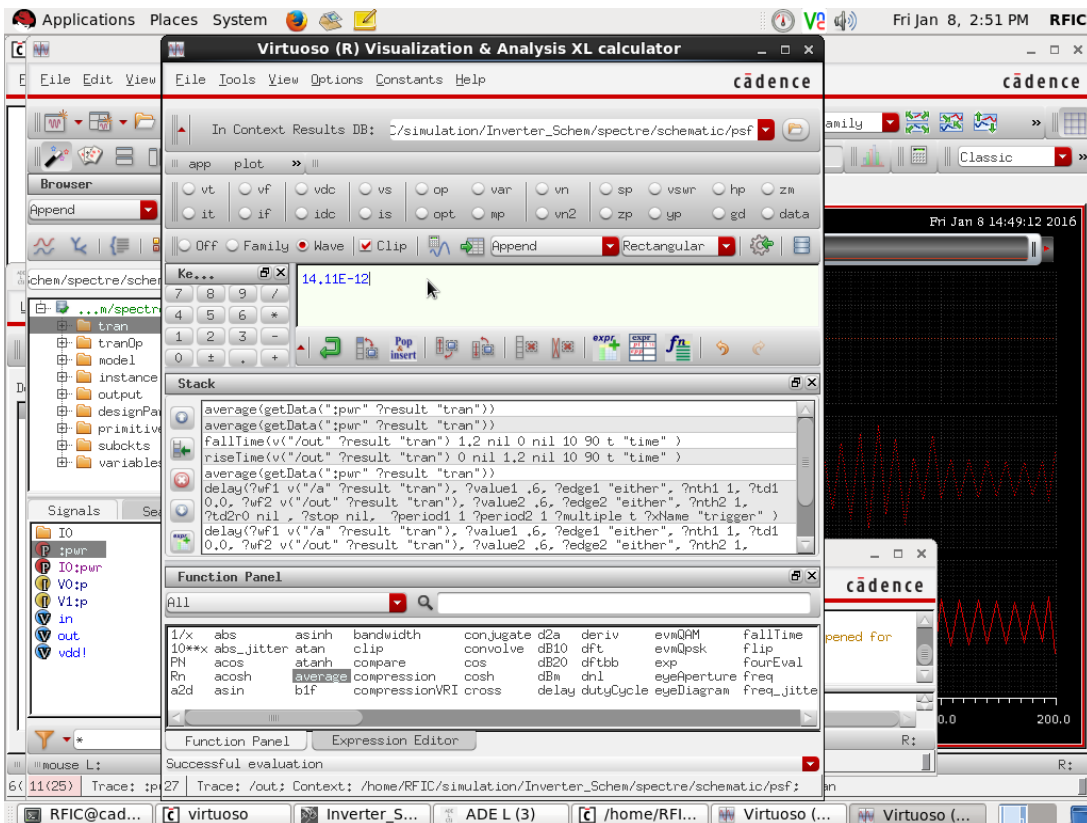


Figure 5 Static power consumption of the Inverter

- Output delays were also calculated using calculator in waveform window. Output rise delay was found as 95p s and output fall delay was found as 108p s.

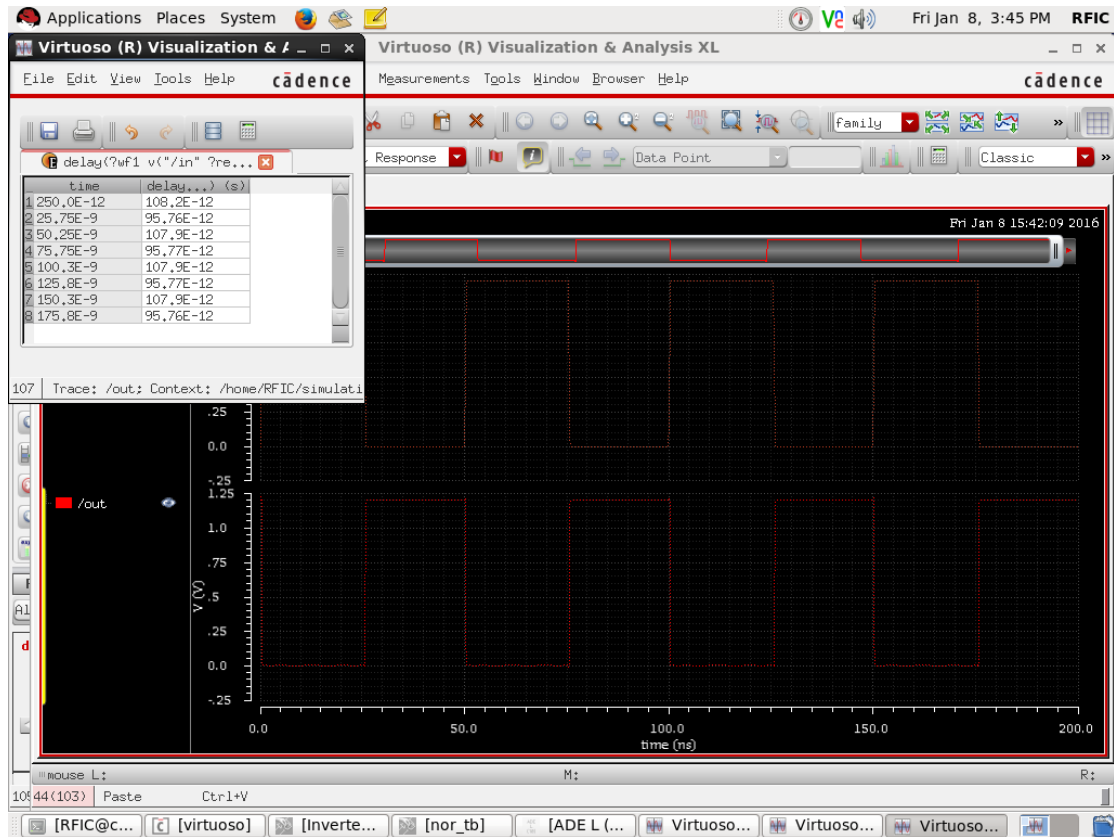


Figure 6 Calculation of Rise delay and Fall delay of Inverter

- Layout was created for the schematic and following tests were conducted
 - DRC
 - LVS

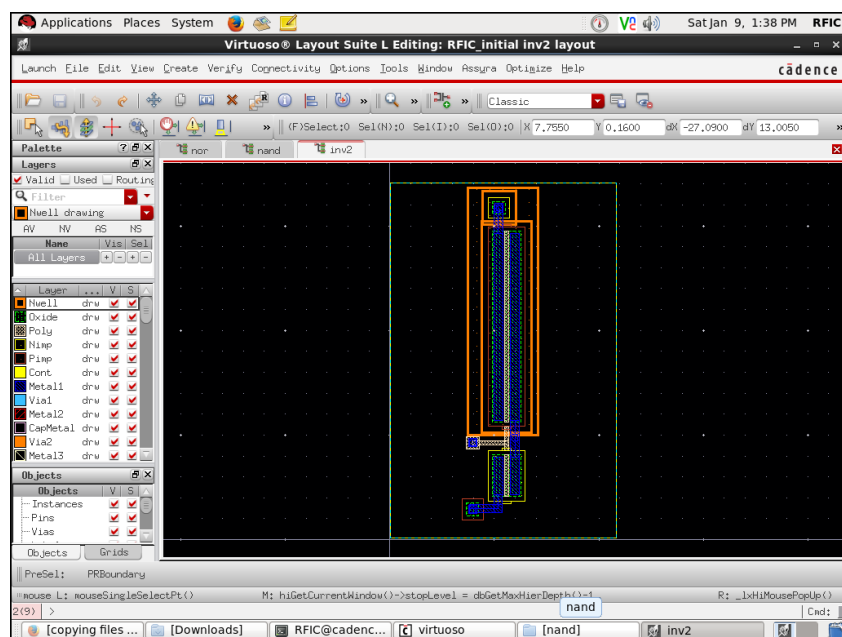


Figure 7 Layout of Inverter

- RC extraction was done for the layout and a netlist was created to show all the resistance and capacitance values in the extracted view.

```
// Generated for: spectre
// Generated on: Jan 7 12:50:48 2016
// Design library name: RFIC_initial
// Design cell name: INVERTER
// Design view name: av_extracted
simulator lang=spectre
global 0 vdd1
include "/home/cadence_ws_labs_614/models/spectre/gpdk.scs" section=stat

// Library name: RFIC_initial
// Cell name: INVERTER
// View name: av_extracted
c1 (a 0) capacitor c=2.553e-16
c2 (y 0) capacitor c=1.935e-16
c3 (N2\ia 0) capacitor c=5.049e-16
c4 (N1\ia 0) capacitor c=1.935e-16
c5 (N1\iy 0) capacitor c=2.644e-16
c6 (N1\ydd1 0) capacitor c=1.049e-16
c7 (N5\ydd1 0) capacitor c=1.067e-17
c8 (N2\iy 0) capacitor c=9.257e-16
c9 (N3\ydd1 0) capacitor c=8.627e-16
c10 (N3\ia 0) capacitor c=2.448e-16
r1 (N1\gnd1 N3\gnd1) resistor r=2.2457 c=0
r2 (N3\gnd1 0) resistor r=0.003704 c=0
r3 (N2\gnd1 N3\gnd1) resistor r=7 c=0
r4 (vdd1 N2\ydd1) resistor r=0.00122 c=0
r5 (N2\ydd1 N4\ydd1) resistor r=0.9214 c=0
r6 (N4\ydd1 N5\ydd1) resistor r=1.1163 c=0
r7 (N5\ydd1 N6\ydd1) resistor r=7.7633 c=0
r8 (N1\ydd1 N2\ydd1) resistor r=7 c=0
r9 (N3\ydd1 N4\ydd1) resistor r=0.6364 c=0
r10 (N3\ydd1 N5\ydd1) resistor r=0.6364 c=0
r11 (N2\iy N1\iy) resistor r=2.3763 c=0
r12 (y N1\iy) resistor r=1.0063 c=0
r13 (N2\iy N2\iy) resistor r=1.7526 c=0
r14 (N2\iy N3\iy) resistor r=0.6364 c=0
r15 (N2\ia N3\ia) resistor r=70.0901 c=0
r16 (N3\ia a) resistor r=10.376 c=0
r17 (N3\ia vdd1) resistor r=61.1317 c=0
PM0 (N2\iy N2\ia N3\ydd1 N1\ydd1) pmos1 w=9.125e-06 l=1.8e-07 as=5.475p \
ad=5.475p ps=19.45u pd=19.45u n=(1)*(1)
NM0 (N1\iy N4\ia N1\gnd1 N2\gnd1) nmos1 w=2e-06 l=1.8e-07 as=1.2p \
ad=1.2p ps=5.5u pd=5.5u n=(1)*(1)
simulatorOptions options reitole=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
trow=27 scales=1 scale=1.0 gain=1e-12 rforce=1 naxnotes=5 maxwarns=5 \
digits=5 cols=80 pivrel=1e-3 sensfiles="..\psf\sens.output" \
check11a1dest=psf
```

Figure 8 Netlist creation of the Inverter

- Post layout simulation was done and the above parameters were calculated again and tabulated in the following table.
- The following are the screenshots of the tests done to the NAND and NOR gates.

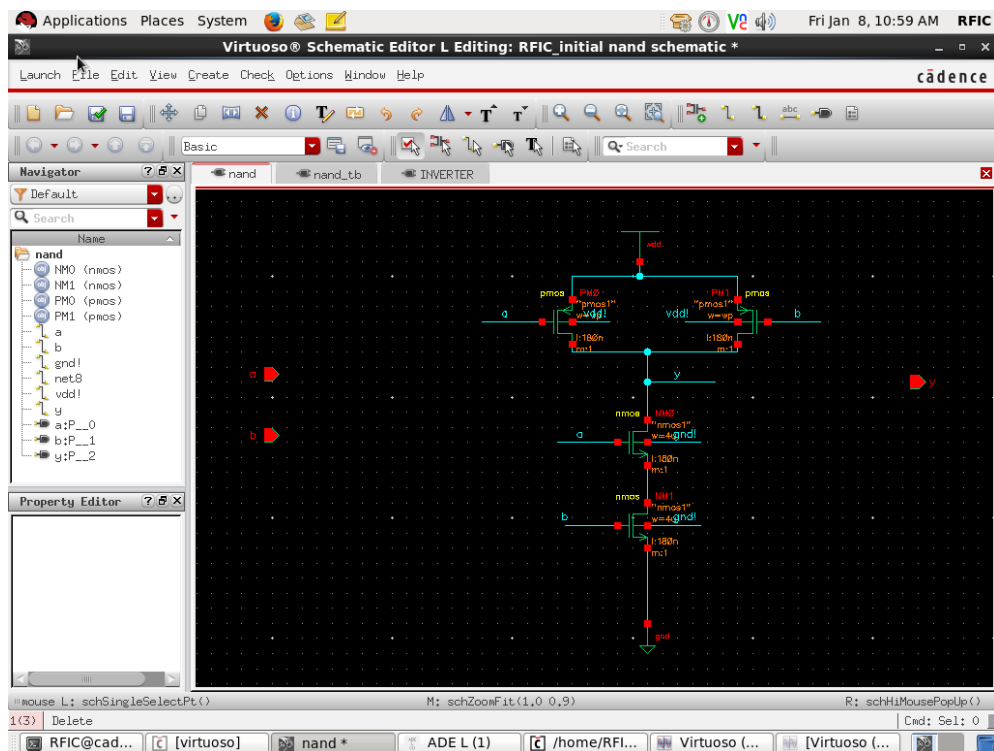


Figure 9 Schematic of NAND gate

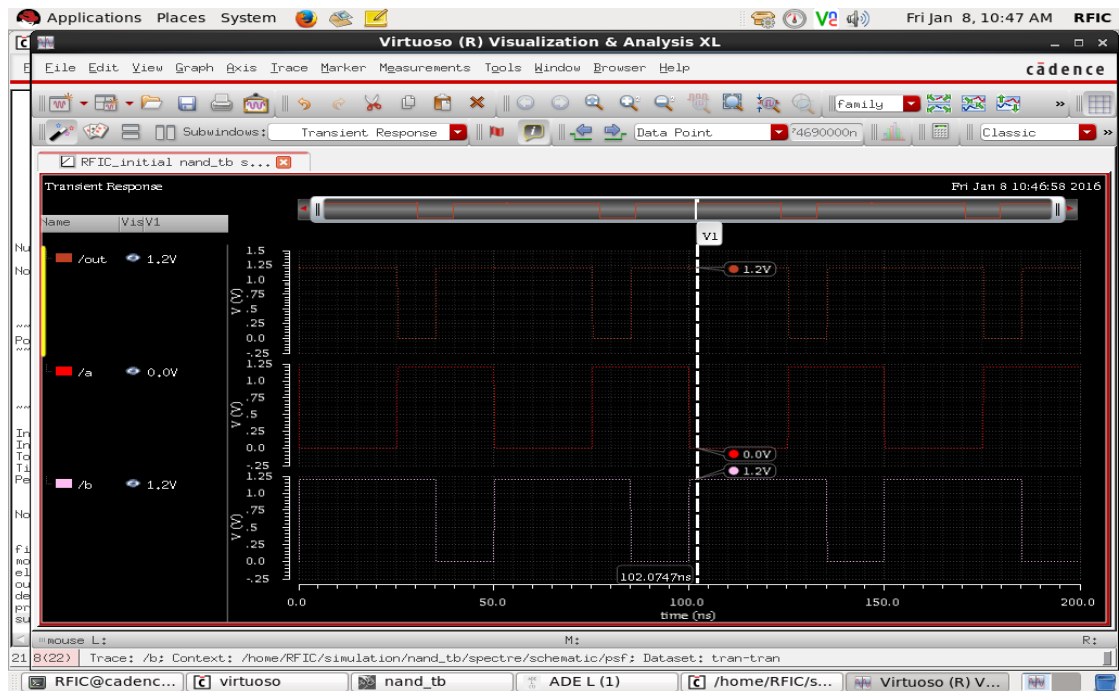


Figure 10 NAND Functionality check

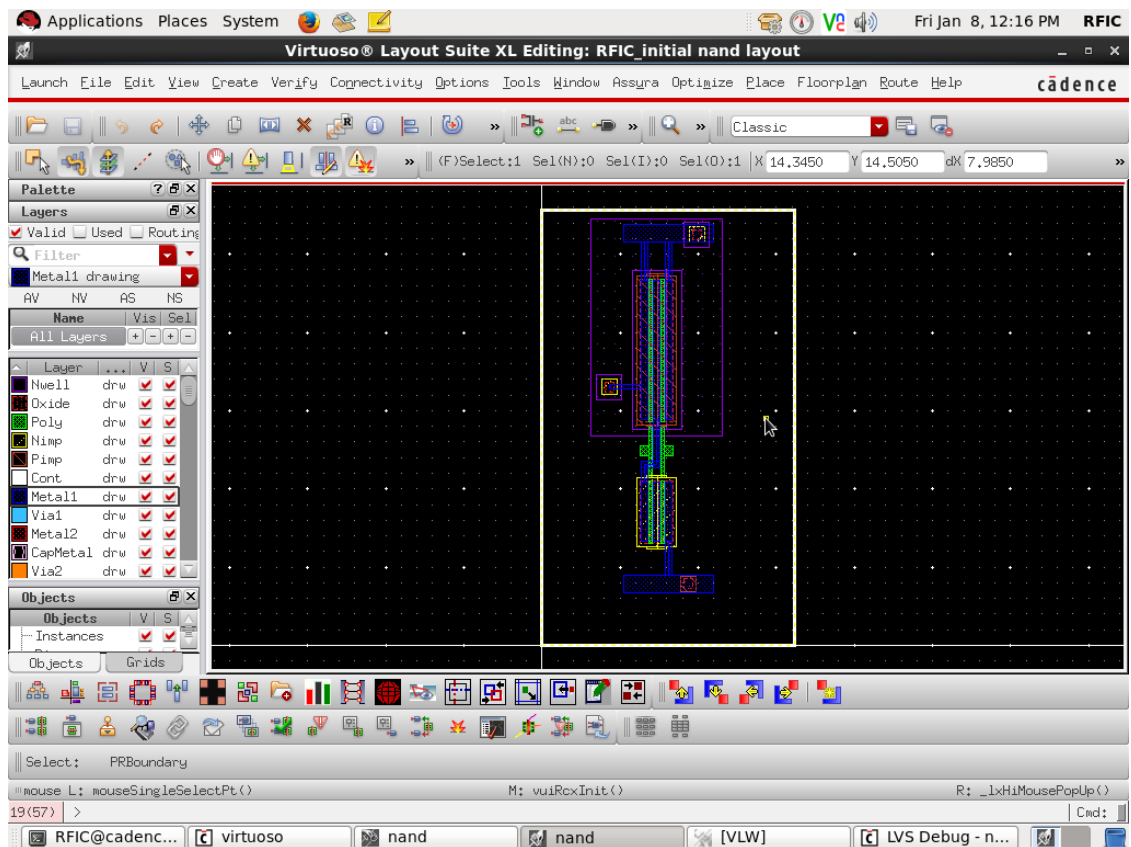


Figure 11 Layout of NAND gate

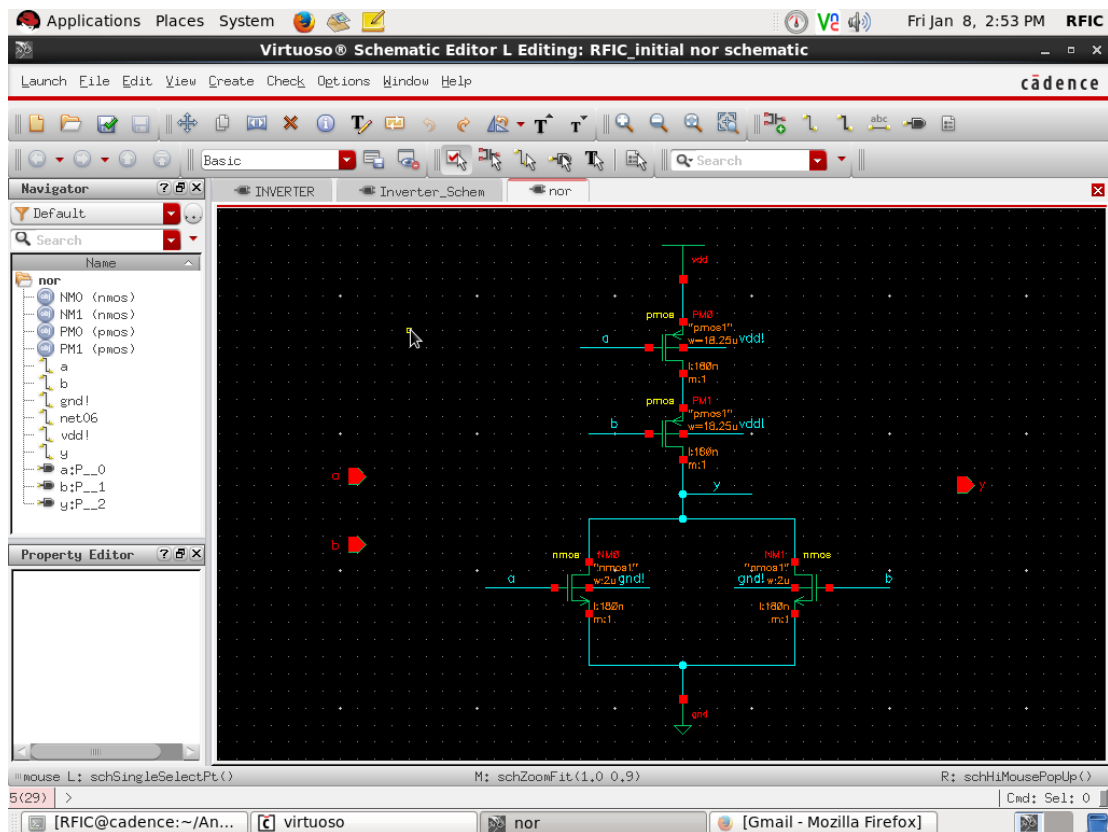


Figure 12 Schematic of NOR gate

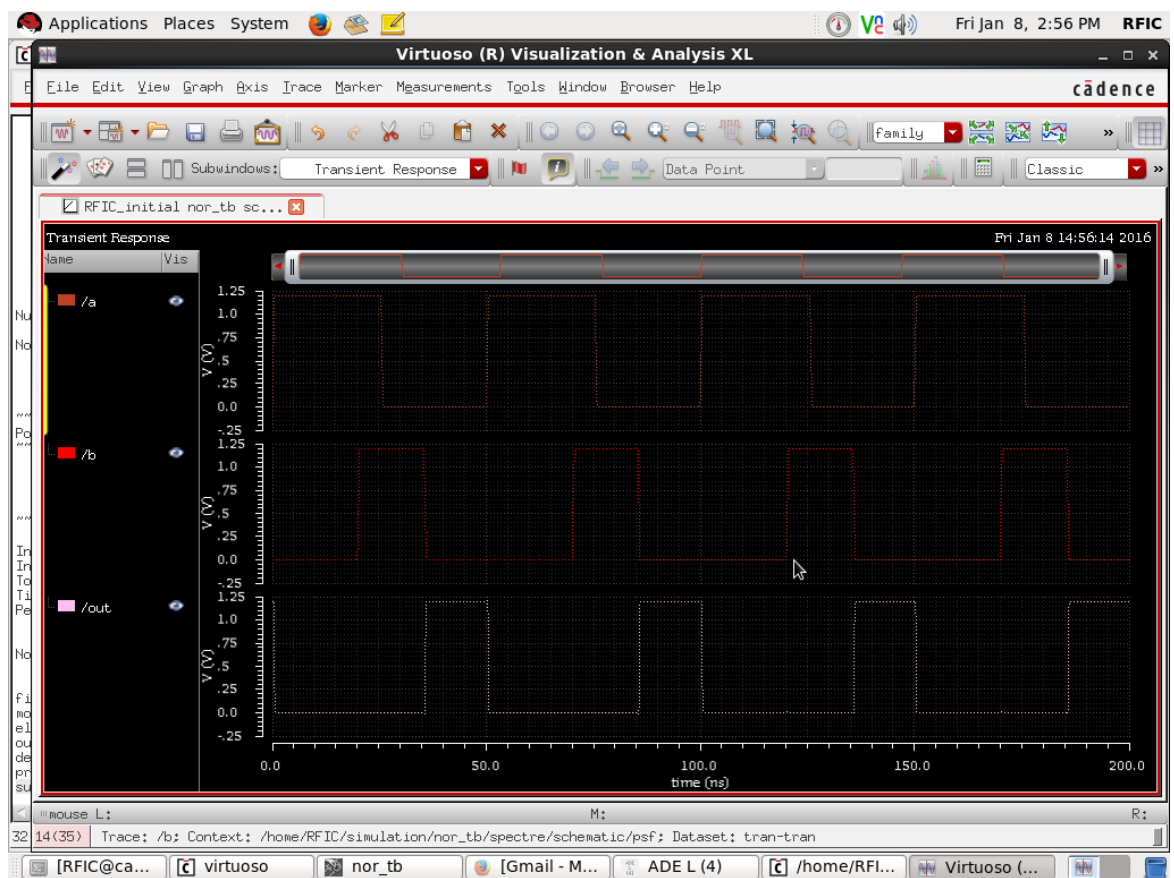


Figure 13 NOR gate functionality test

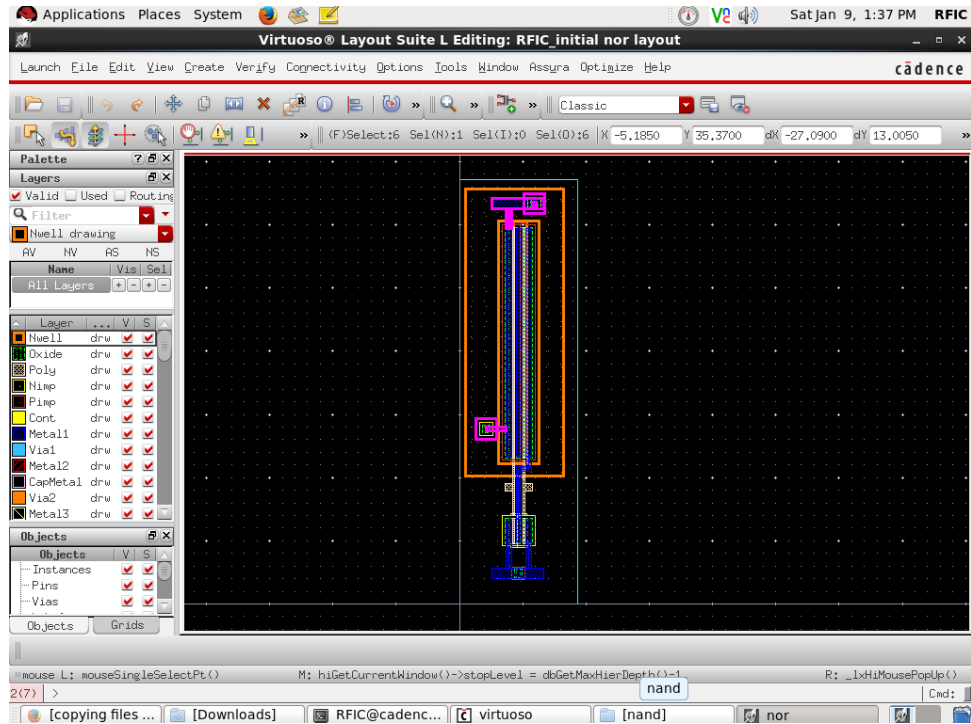


Figure 14 Layout of NOR gate

Results:

- The results are tabulated below.

Table 1 Parameters of the Inverter

Parameters	Pre-Layout Simulation	Post-Layout Simulation
Rise Time(s)	101p	105p
Fall Time(s)	95p	100p
Total Power(W)	576.7n	625n
Static Power(W)	14.11p	14.11p
Rise Delay(s)	95p	101p
Fall Delay(s)	108p	112p

- Similar process was carried out for NAND and NOR gates too and the results are tabulated below.

Table 2 Parameters of NAND gate

Parameters	Pre-Layout Simulation	Post-Layout Simulation
Rise Time(s)	130p	133p
Fall Time(s)	124p	125p
Total Power(W)	1.086u	1.2u
Static Power(W)	5.758p	7.5p
Rise Delay(s)-A	131p	132p
Fall Delay(s)-A	130p	130p
Rise Delay(s)-B	155p	155p
Fall Delay(s)-B	135p	135p

Table 3 Parameters of NOR gate

Parameters	Pre-Layout Simulation	Post-Layout Simulation
Rise Time(s)	130p	133p
Fall Time(s)	124p	125p
Total Power(W)	1.086u	1.2u
Static Power(W)	5.758p	7.5p
Rise Delay(s)-A	131p	132p
Fall Delay(s)-A	130p	130p
Rise Delay(s)-B	155p	155p
Fall Delay(s)-B	135p	135p