Aim: To design an inverter, nand & nor and perform the following operations

1) Schematic simulation
2) Calculation of rise time, fall time, delay, power consumption.
3) Creation of layout and performing DRC, LVS and RCX.
4) Performing post layout simulation

Procedure:

- A schematic was done for the inverter and its functionality was verified.

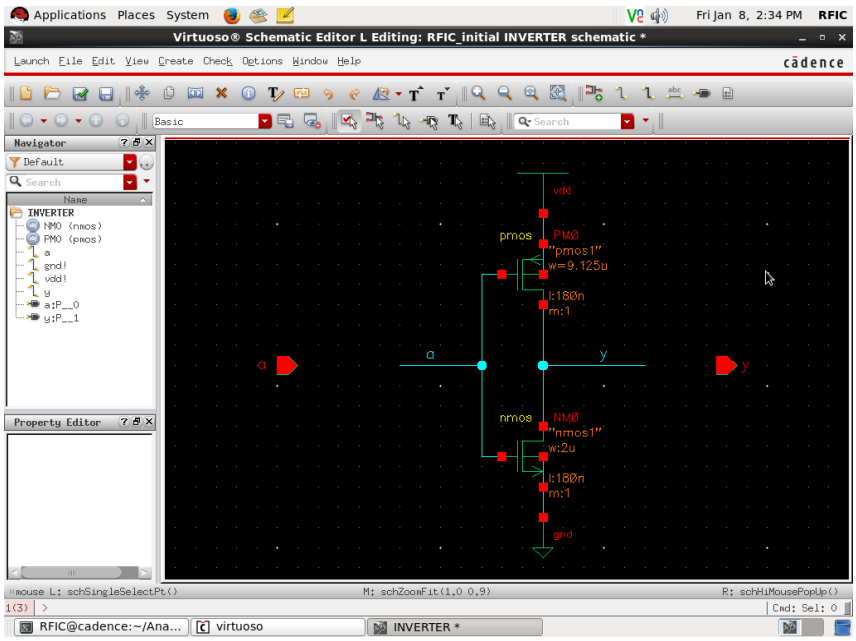

Figure 1 Schematic of Inverter

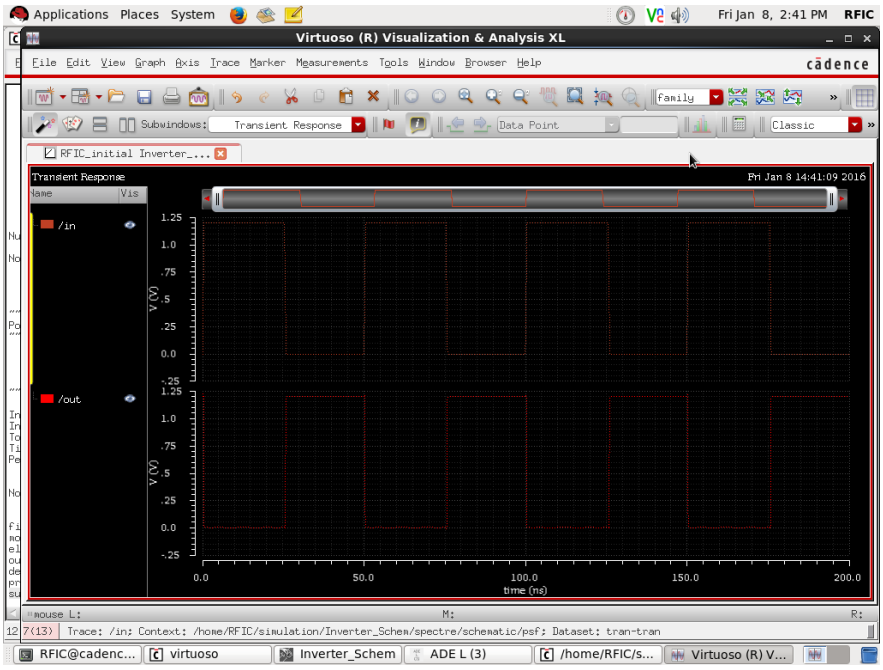

Figure 2 Functional verification of Inverter

- Sizing was done so that the switching threshold was half of V_{dd} and it was made sure that rise and fall times of the outputs are nearly equal. W_n was decided to be 2u and W_p as 9.1255u.
- Output rise and fall times were calculated to be 101p s and 95p s respectively, when input rise and fall times were both kept at 500p s. These were done using the rise and fall time functions in the calculator.

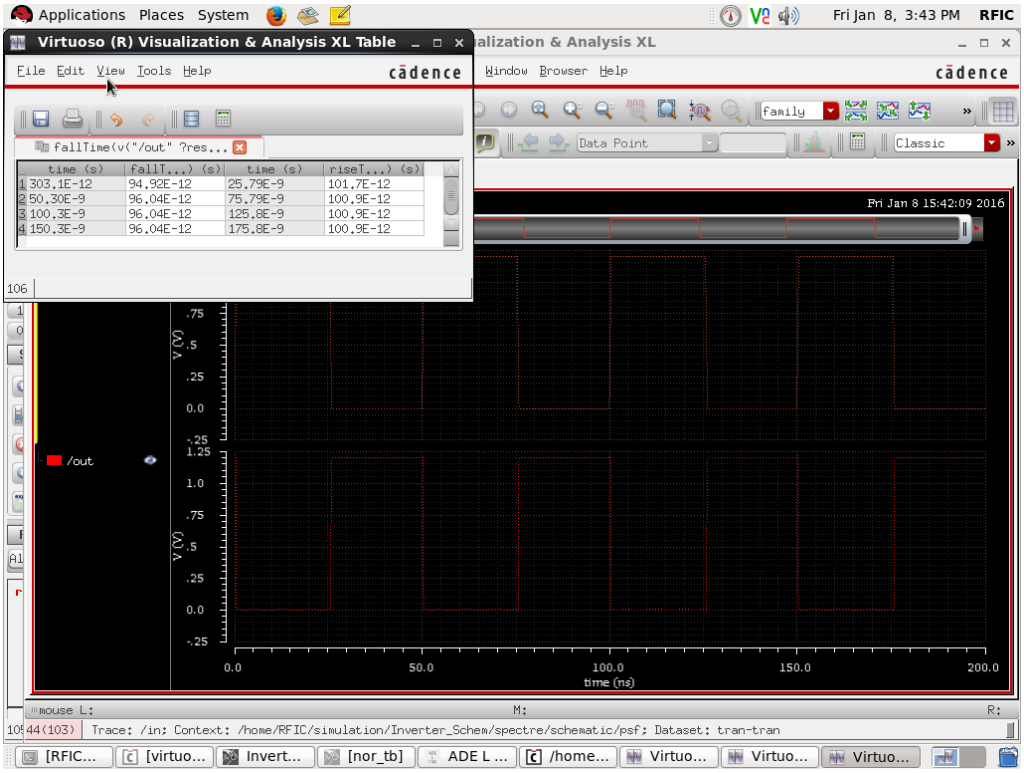

Figure 3 Calculation of rise time and fall time of the Inverter

- Average power consumption was calculated as 576.7n W. Static power dissipation was found by making sure that there was no switching activity in the circuit and it was found to be 14.11p W.

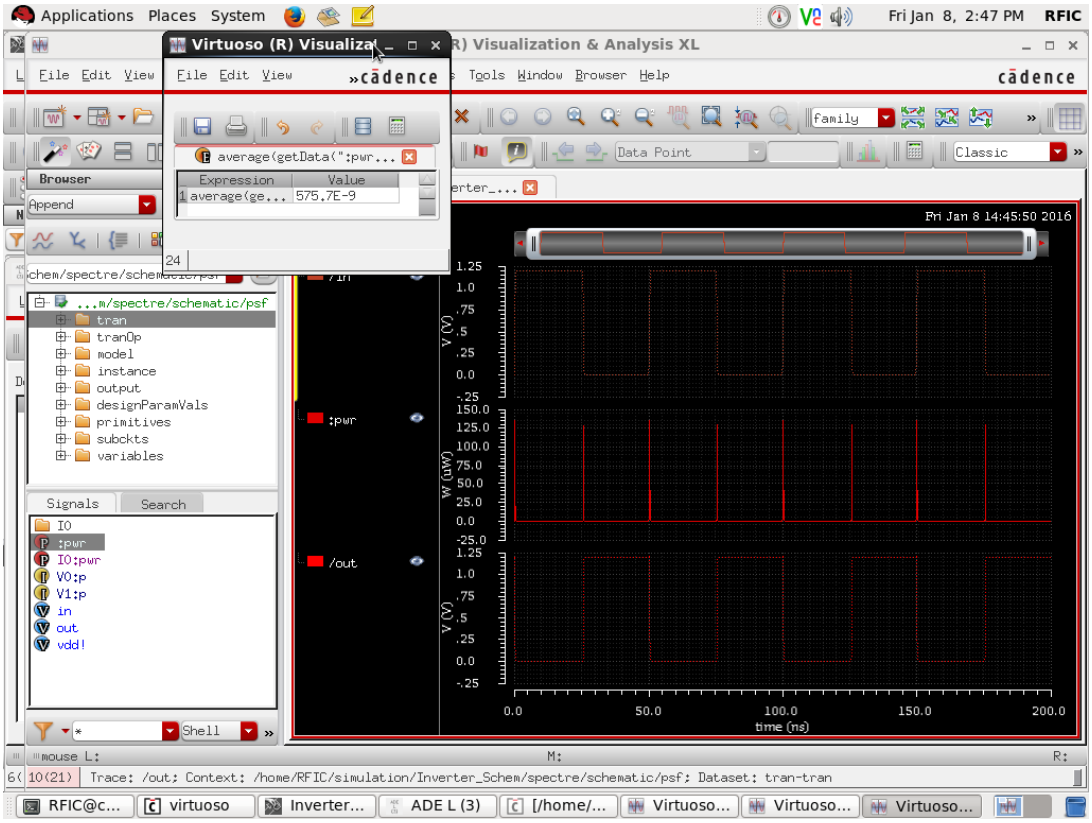

Figure 4 Total power consumption of the Inverter

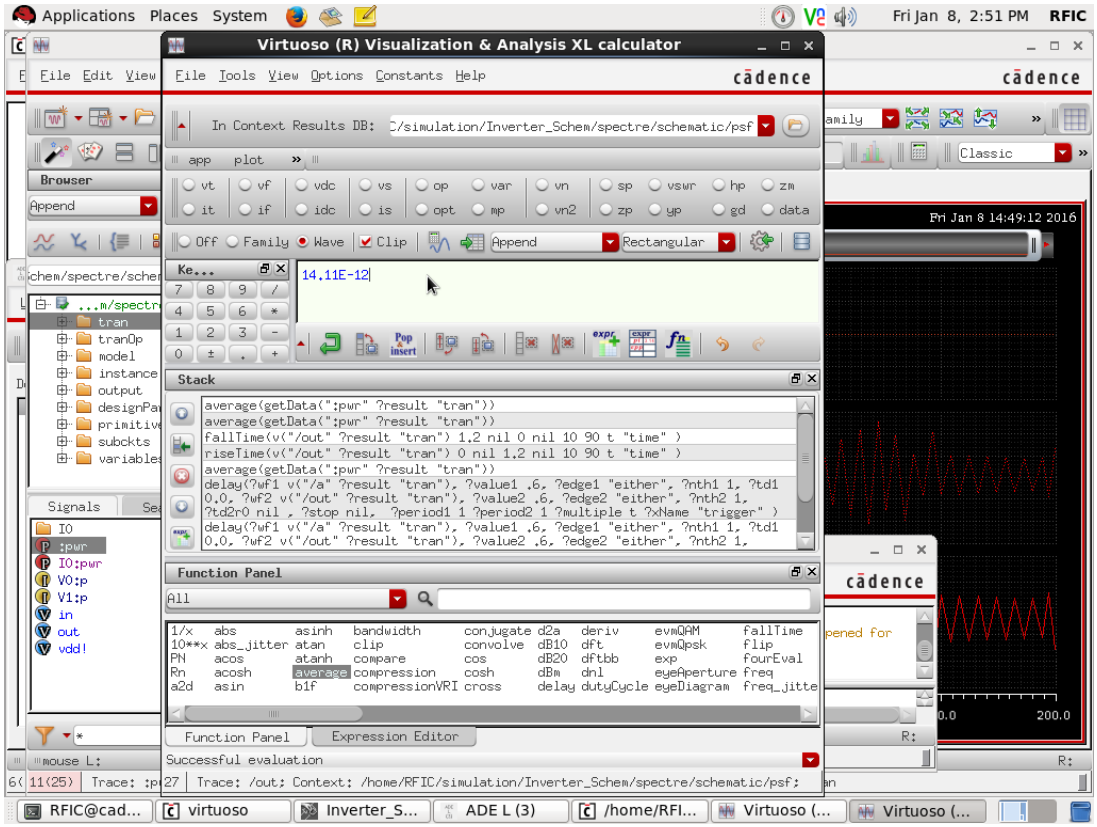

Figure 5 Static power consumption of the Inverter

- Output delays were also calculated using calculator in waveform window. Output rise delay was found as 95p s and output fall delay was found as 108p s.

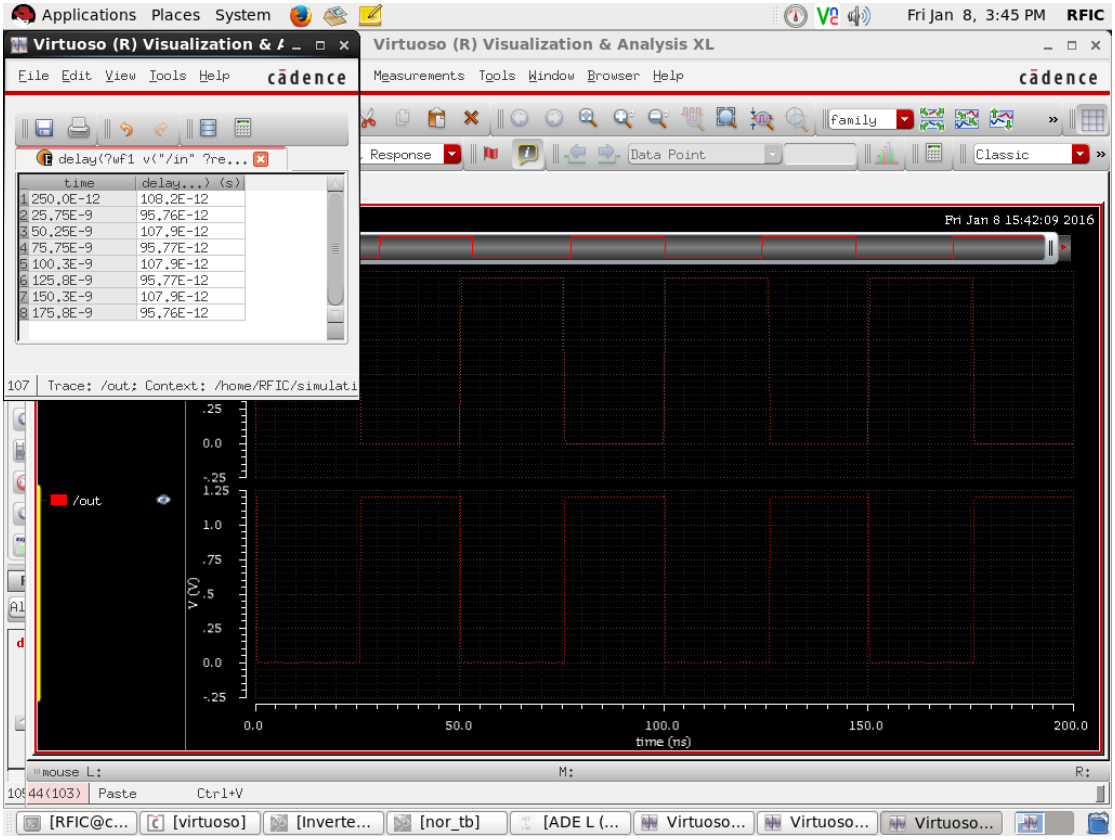

Figure 6 Calculation of Rise delay and Fall delay of Inverter

- Layout was created for the schematic and following tests were conducted
  - DRC
  - LVS

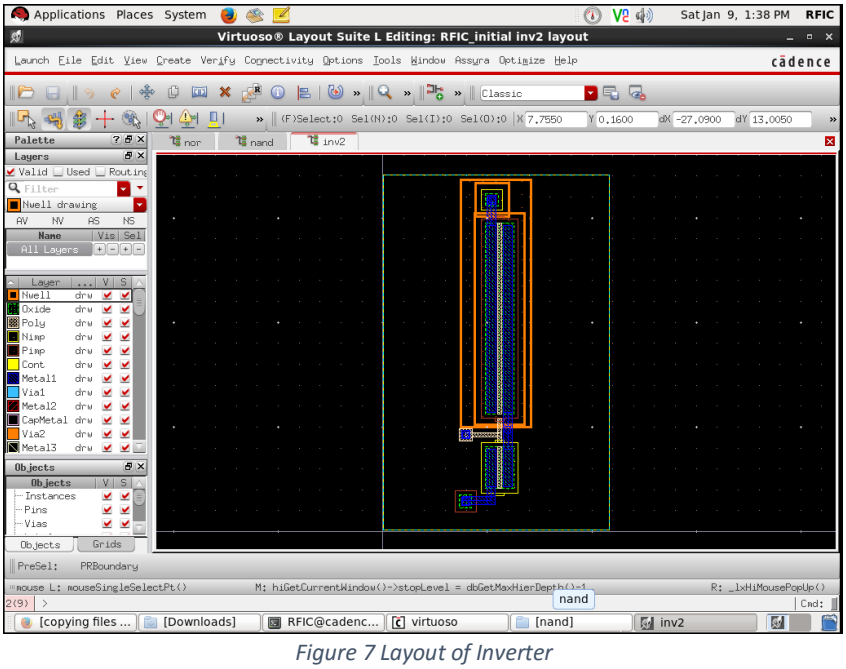

Figure 7 Layout of Inverter

- RC extraction was done for the layout and a netlist was created to show all the resistance and capacitance values in the extracted view.

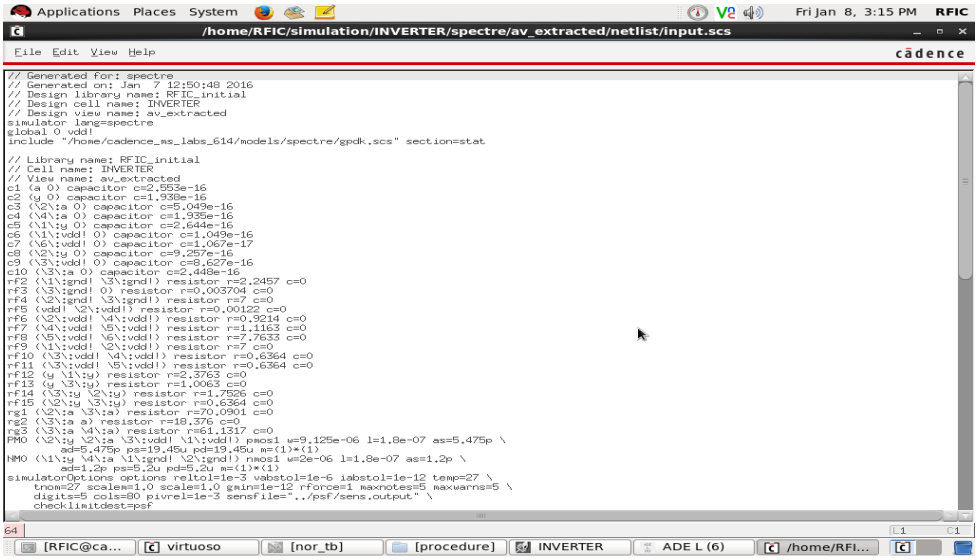

Figure 8 Netlist creation of the Inverter

- Post layout simulation was done and the above parameters were calculated again and tabulated in the following table.

- The following are the screenshots of the tests done to the NAND and NOR gates.

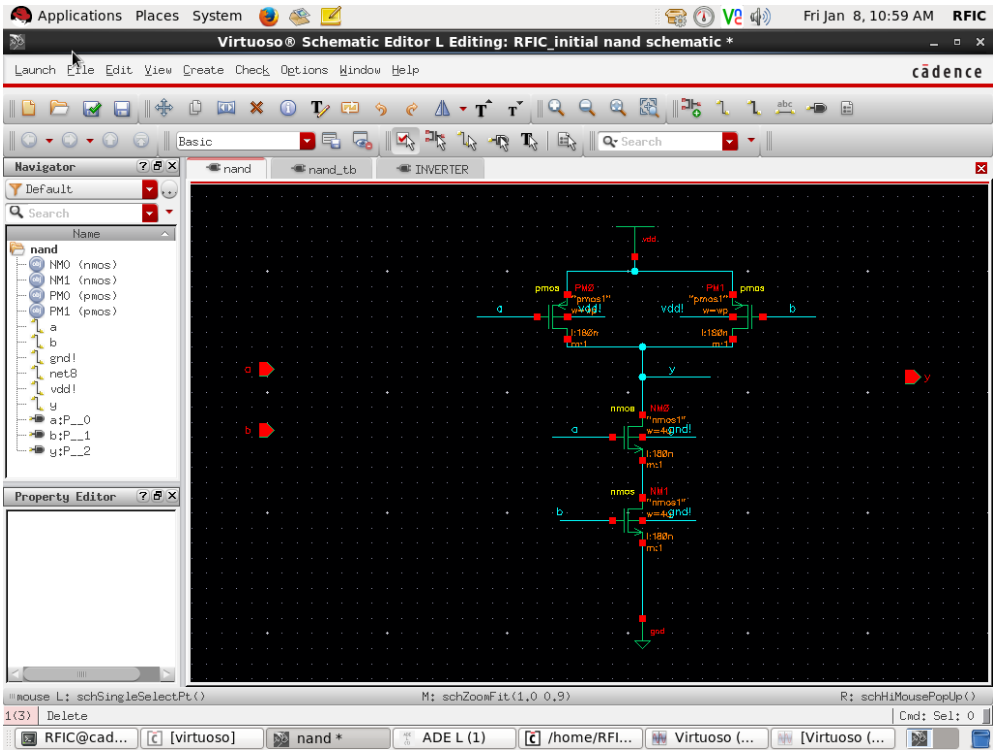

Figure 9 Schematic of NAND gate

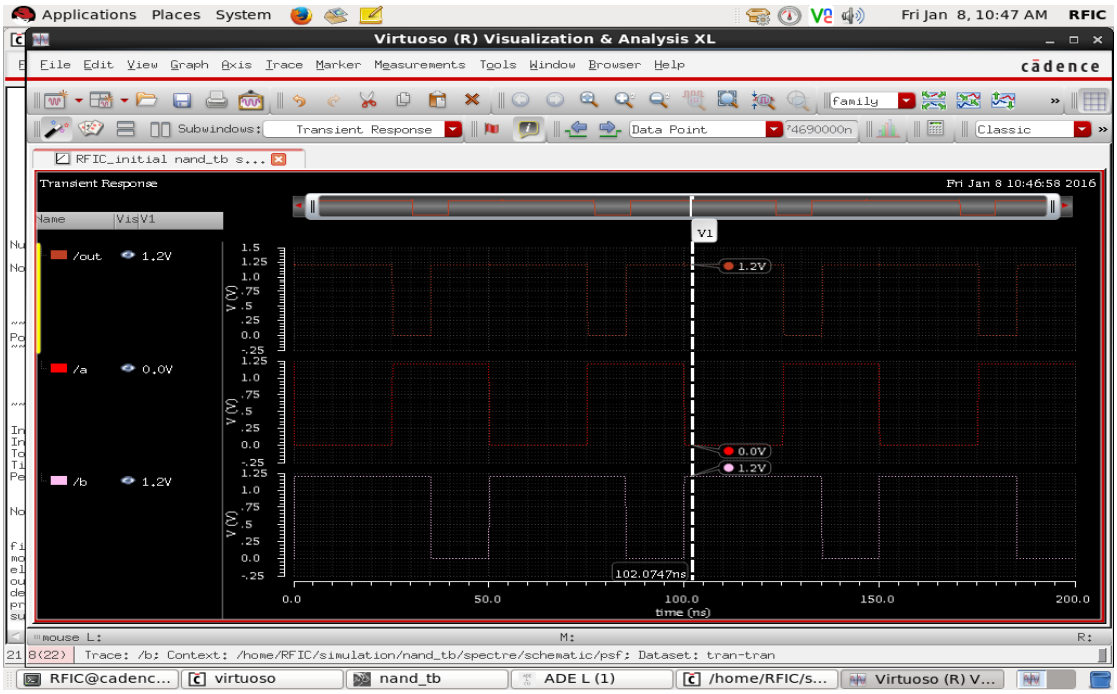

Figure 10 NAND Functionality check

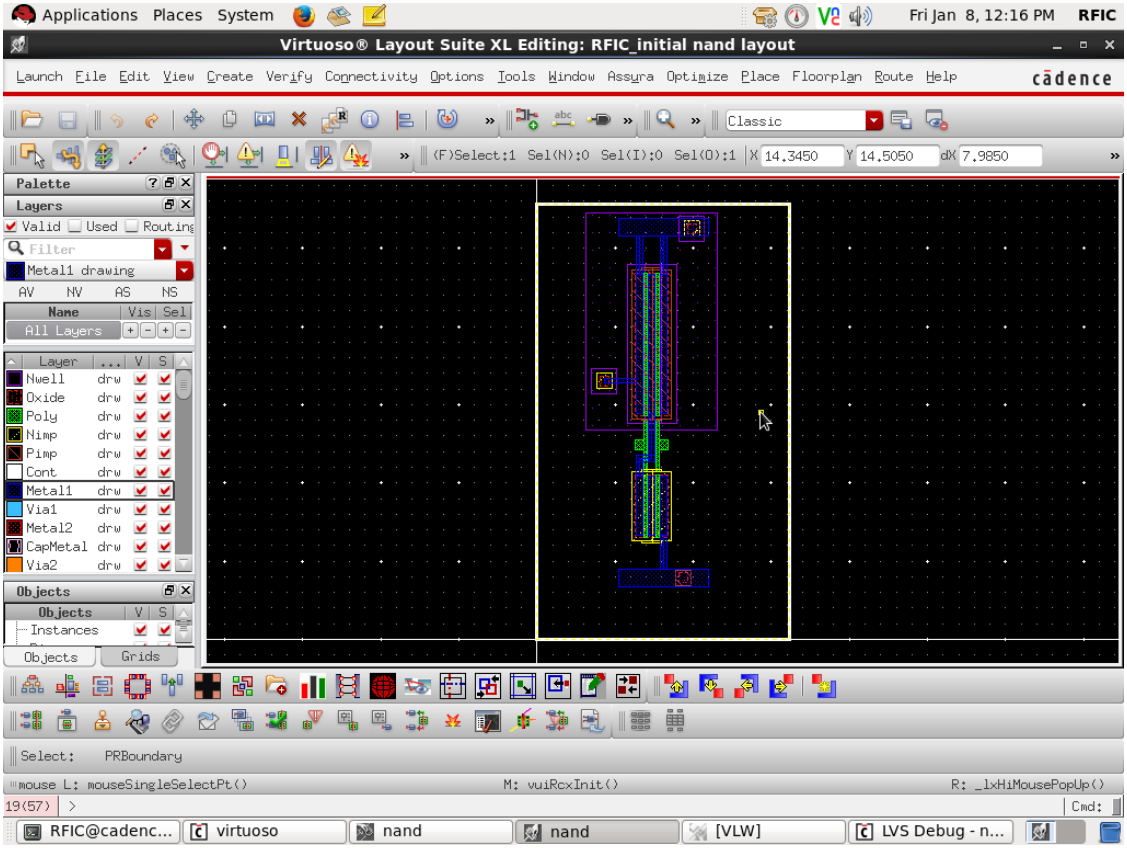

Figure 11 Layout of NAND gate

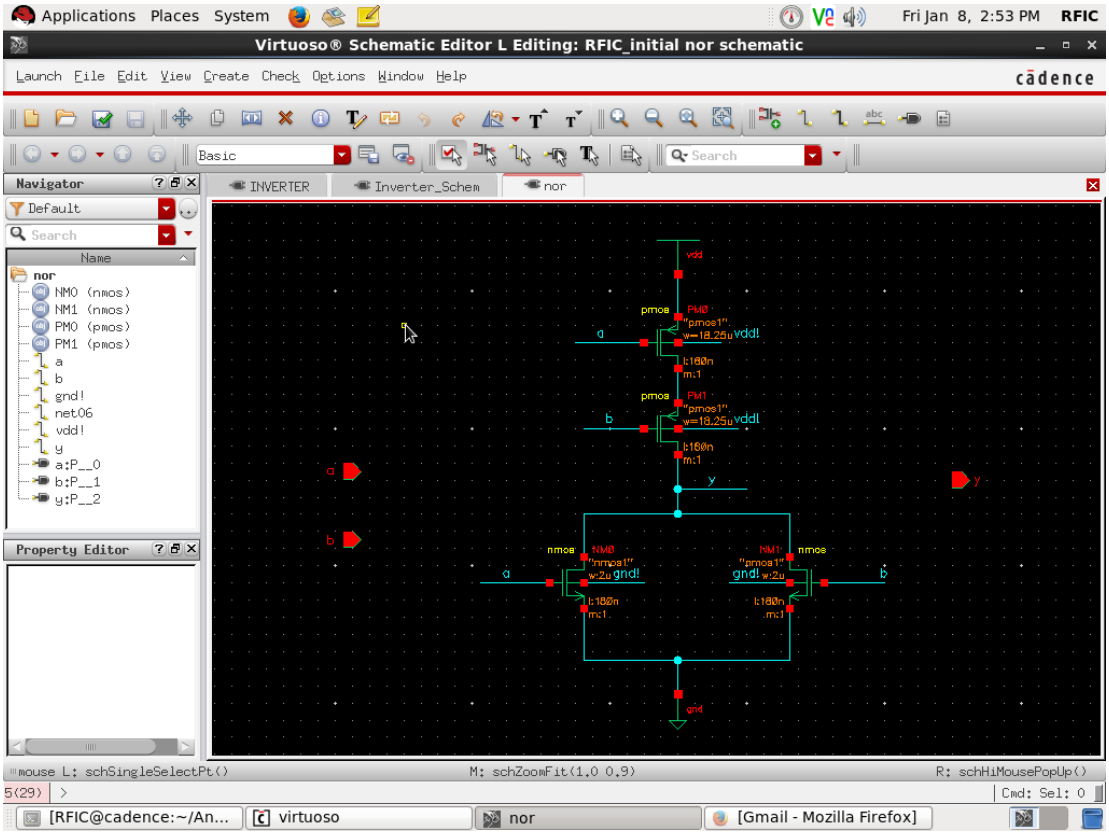

Figure 12 Schematic of NOR gate

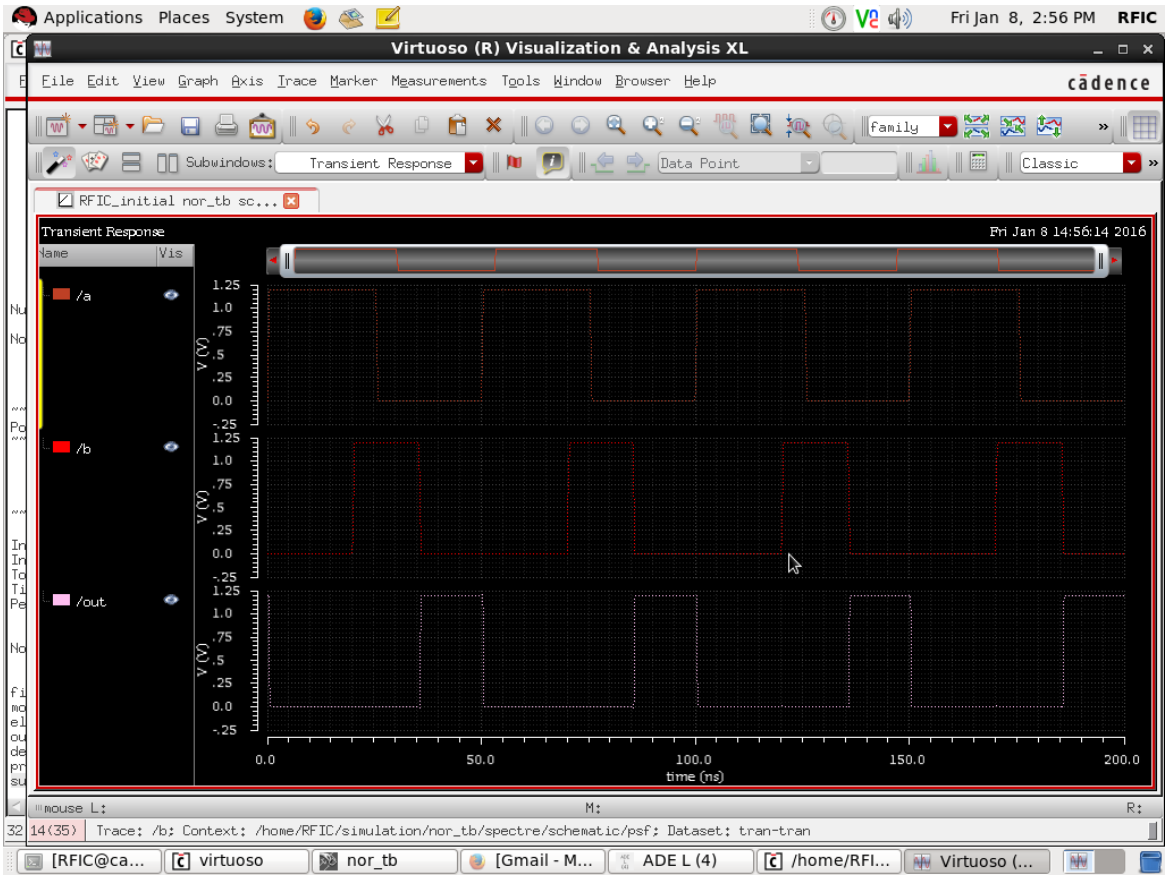

Figure 13 NOR gate functionality test

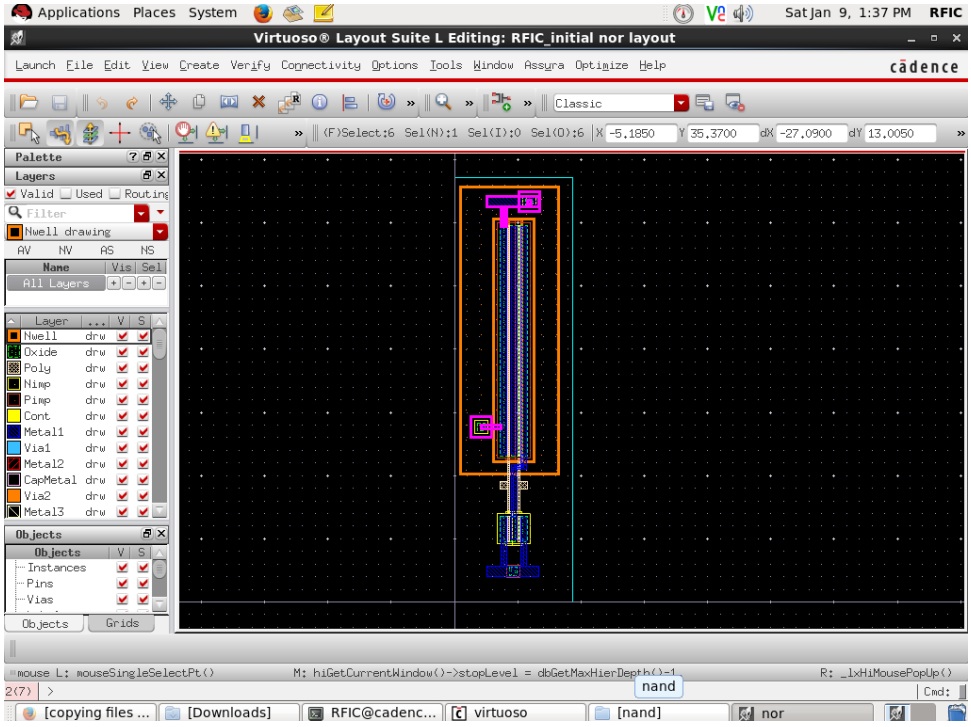

Figure 14 Layout of NOR gate

Results:

- The results are tabulated below.

Table 1 Parameters of the Inverter

Parameters	Pre-Layout Simulation	Post-Layout Simulation
Rise Time(s)	101p	105p
Fall Time(s)	95p	100p
Total Power(W)	576.7n	625n
Static Power(W)	14.11p	14.11p
Rise Delay(s)	95p	101p
Fall Delay(s)	108p	112p

- Similar process was carried out for NAND and NOR gates too and the results are tabulated below.

Table 2 Parameters of NAND gate

Parameters	Pre-Layout Simulation	Post-Layout Simulation
Rise Time(s)	130p	133p
Fall Time(s)	124p	125p
Total Power(W)	1.086u	1.2u
Static Power(W)	5.758p	7.5p
Rise Delay(s)-A	131p	132p
Fall Delay(s)-A	130p	130p
Rise Delay(s)-B	155p	155p
Fall Delay(s)-B	135p	135p

Table 3 Parameters of NOR gate

Parameters	Pre-Layout Simulation	Post-Layout Simulation
Rise Time(s)	130p	133p
Fall Time(s)	124p	125p
Total Power(W)	1.086u	1.2u
Static Power(W)	5.758p	7.5p
Rise Delay(s)-A	131p	132p
Fall Delay(s)-A	130p	130p
Rise Delay(s)-B	155p	155p
Fall Delay(s)-B	135p	135p