सीएसआईआर - केंद्रीय इलेक्ट्रॉनिकी
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CSIR- Central Electronics Engineering Research Institute,
वैज्ञानिक एवं औद्योगिक अनुसंधान परिषद्
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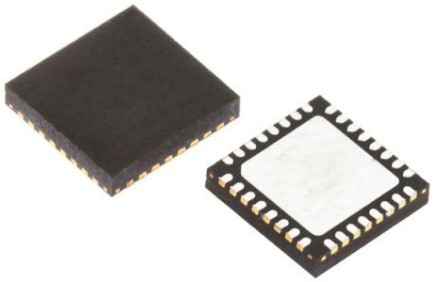
पिलानी-333031, राजस्थान, भारत
Pilani-333031, Rajasthan, India



ASIC3-A

SINGLE CHANNEL ASIC

CEERI, Pilani, Rajasthan, India.

ASIC-3A is a industrial sensor interface chip comparable to gas sensor interface chip OR light sensor interface chip. In one line this chip generates F_SET and F_RESET output as per the input data and the conditional parameters.

ASIC-3A is intended for reception and analysis of input signals and formation of output signals in compliance with the requirement of present specification.

In process of operation ASIC-3A forms the pulses SET at output F_SET and Reset at output F_RESET. parameters of output pulses are determined by the written command from the digital port and signals at analog inputs (COMP_IN and VCO_IN)

In order to check parameters and testASIC-3A there may be used the control signals, formed at outputs { COMP_OUT, SET_ENB, RESET_ENB, DATA_ENB, SYNC_ENB }

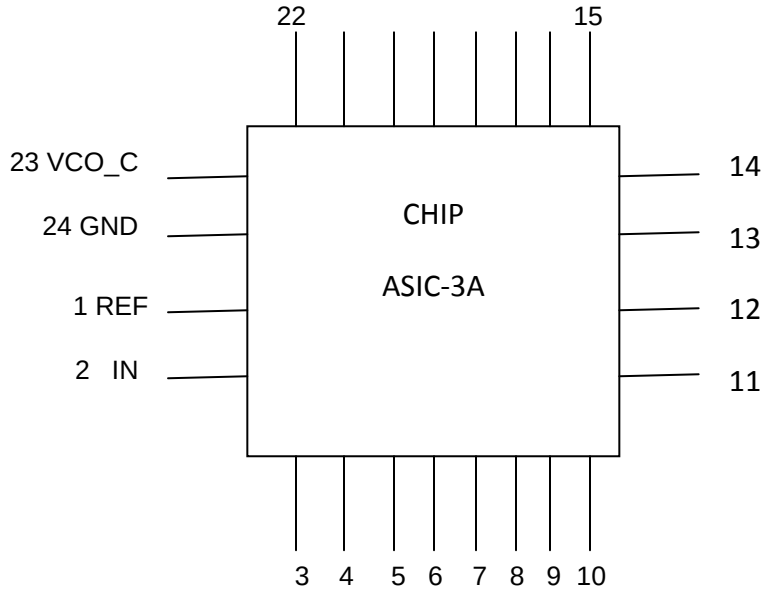
1. Functional block diagram is indicated in Fig 1
2. Pin designations in Table 1
3. time chart of input / output signals is indicated in Fig 2
4. Electric parameters are listed in table 2
5. ASIC-3A is fabricated in package H06.24-1B. Dimension and connection sizes are indicated in Fig.3
6. DC supply voltage range Vcc 6 to 7 V
7. Range of output currents 1 to 10 mA
8. Serial inputs for 8 bit

9. Logic levels at inputs in compliance with table 2
10. All digital inputs have schmitt triggers
11. ASIC-3A does not respond to signals at digital serial inputs, if their duration is less than 250ns
12. Pulse duration Load at input { E/L } is set by means of oscillation application of internal frequency.
13. Pulses required for formation of output pulse { F_SET } formed by the built in voltage controlled oscillator as indicated in fig 1
14. ASIC-3A maximum switch rate constitutes 4kHz
15. VCO is developed with consideration that the time setting capacitor C is thermally stable.
16. Delay between the fall edge of pulse LOAD at input { E/L } and rise edge of pulse SET at output {F_SET } is within the limits indicated below

    Minimum delay - 6 periods of VCO frequency ; maximum delay- 7 periods of VCO frequency

17. Range of operating temperature Ta = -55 to 125 degree centigrade
18. Storage temperature range Ts = -65 to 150 degree centigrade
19. Sensitivity to electrostatic discharge 500V (in compliance with MIL-STD 883 E method 3015.7)
20. Microcircuit is intended for application by the standard MIL-STD 810 C (B). Test methods and procedures are in compliance with standard MIL-I-38535 group {A}, {C}, { D (subgroup 4) } and MIL-883C
21. marking is in compliance with the requirement of the appropriate provision.

Table 1. Designation of pins



Designation	Function	Pin No
REF	Comparator analog input	1
IN	Comparator analog input	2
COMP_OUT	Comparator output	3
RESET	Output	4
MONO-C1	External Capacitor	5
MONO-C2	External capacitor	6
VCO-RV	External Resistor	7
VCC	Supply Voltage	8
NC	No Connection	9
E/L	Digital Input	10
DATA	Digital input	11
SYNC_ENB	Output	12
POR	Reset input	13
SET_ENB	Output	14
SET	Output	15
RST_ENB	Output	16
DATA_ENB	Output	17
GND	Ground	18
VCO_OUT	Input/ Output	19
VCO_IN	Analog input	20
VCO_R	External Resistor VCO	21
CONTROL_PAD	Output permission input	22
VCO_C	External capacitance VCO	23
GND	Ground	24

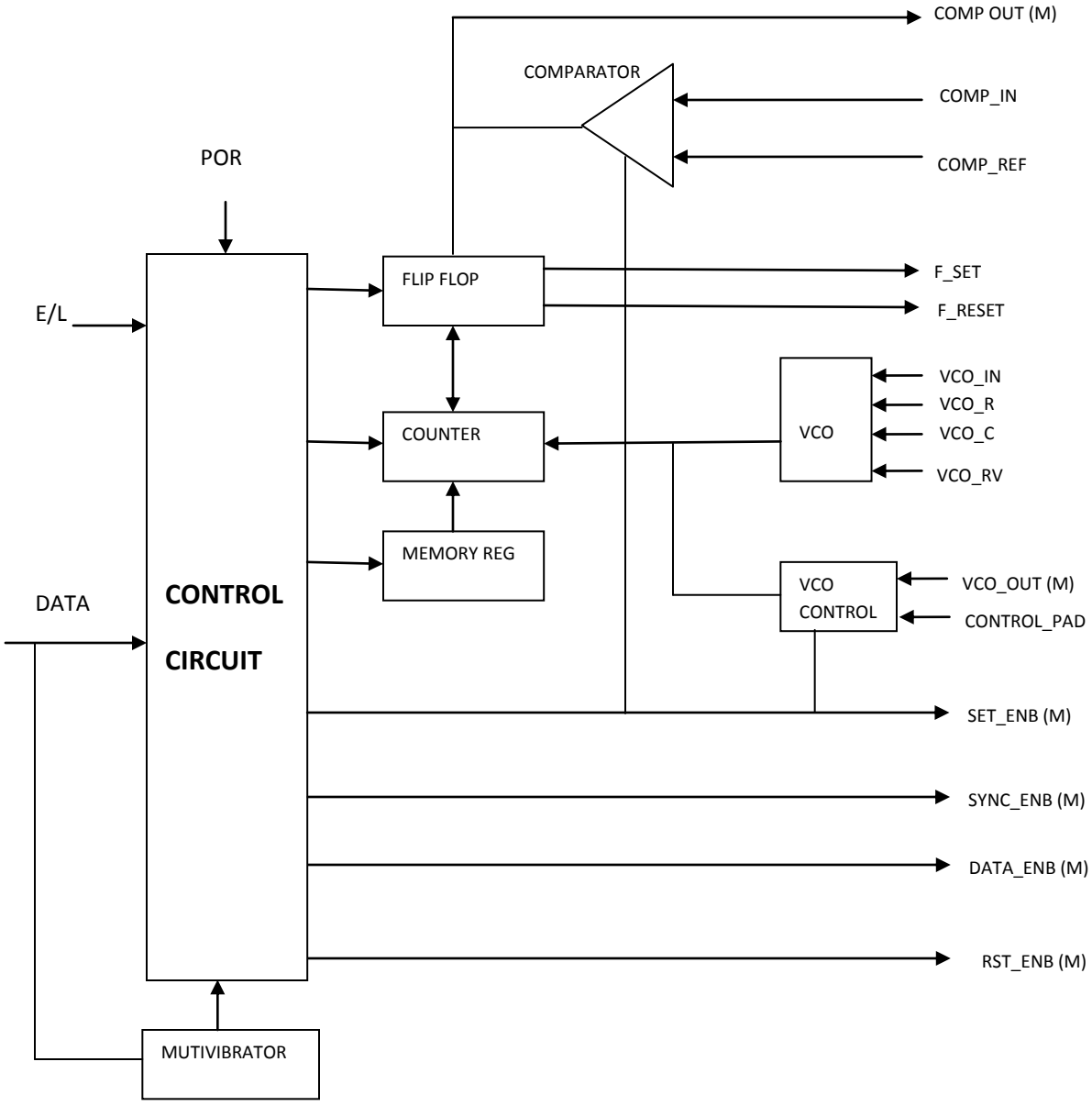


Fig 3 : Block diagram ASIC -3

SCHEMATIC TECHNICAL DESCRIPTION

Circuit consists following blocks:

Multi vibrator is intended for detection of conditions for start-up of data reception in the serial register. Parameters of pulse synchronization at output DATA are set by the external capacitors, connected to MONO-C1 and MONO-C2

Shift register is intended for the serial writing and storage of 8 bit data.

Comparator is intended for comparison of signals at input { Comp_IN } , { Comp_REF } for termination of output { F_RESET }. Comparator is enabled into the consumption status by the high level at output { SET_ENB }

Voltage controlled oscillator (VCO) generates the cycle pulses for the counter. Oscillator is enabled by means of output { SET_ENB }. oscillator frequency is set by the external elements , connected to pins VCO_C , VCO_R, VCO_RV, and VCO_IN

Counter generates the output signal F_SET after a delay equal to 6/7 periods after the fall edge of the pulse { LOAD } at the input E/L. Duration of Ts signal F_SET is set by the frequency period, generates by VCO and DATA written into shift register.

Control circuit generates the preset signal ASIC (R). Preset signal is generated in the following cases:

- By POR high level
- After completion of the circuit operating cycle by means of the pulse fall edge at output F_SET
- in case of erroneous reception of the senior data bit D7 { Senior bit D7 (SET_ENB)=0 } after completion of 8 cycle reception periods (oscillator).
- In case of pulse absence at input E/L during 2,4 us +/- 15 % after appearance of pulse SYNC_ENB as in case of the short pulse generation SYNC_ENB detection of the start conditions by means of input E/L is denied during 8 to 12 us
- In the event of recording zero in the counter by means of back front of the 7th pulse of the vco.
- At the moment of the pulse execution DATA_ENB , if the duration of the pulse low or high level at the input E/L exceeds 2.4 us +/- 15%.

CIRCUIT PERFORMANCE

Circuit performs in the following way

At the high signal level POR , the ASIC-3A control circuit generates the preset enabling signal into the initial status.

After resetting POR, signal from inputs DATA and E/L arrive into the PULSE DURATION DISCRIMINATOR block, which checks the signal duration at inputs DATA and E/L. If the duration of the serial input signals is over 250ns, then multi vibrator circuit during usage of MONO_C1 and MONO_C2 detects the pulse SYNC at input DATA and generates at time of disabling (T2) after detection of the start pulse at input SYNC_ENB a pulse duration of 2us, set by external capacitance at input MONO-C2. This pulse in the line SET_ENB is synchronized with DATA and the first cycle period of oscillator in line E/L generates the signal Estr, enabling reception of the serial data into the shift register after the pulse duration at output SET_ENB extends from 2us to the fall edge F_SET.

By the rise edge of the first cycle period of signal at input E/L, control signal SET_ENB switches over from low to high and appropriately the level at the control point DATA_ENB switches over from low to high.

In the first cycle period at input E/L is missing, then the signal Estr is not generated. and the remaining 7 cycle periods are not permitted for writing into the subsequent shift register and the pulse duration at output SYNC_ENB is limited by 2us. This ensures ASIC-3A response only for a appropriate start pulse and neglecting other similar pulses at input DATA , which arrive prior and after the margins of actual data.

Information at input DATA is received in the following order:

D7 (SET_ENB) , D6, D5, D4, D3, D2, D1, D0. After completion of 8 cycle reception periods the shift register gets closed. With the reverse edge of the 8th cycle period at input E/L, the control signal at output DATA_ENB switches over from the high to low status, and the control signal at output RESET_ENB switches over from the low to high status.

If D7 (SET_ENB)=0 is received, after reception completion, the control circuit generates the preset signal { R } and the new reception starts after the repeated operation of the multi vibrator.

If D7 (SET_ENB)=1 is received, after reception completion, the pulse LOAD at input E/L is detected for its minimum width of 20us and then the data from the shift register are rewritten into the counter.

Comparator is enabled into the consumption status by means of a signal at output SET_ENB. The comparator output is strobed by the signal, which is generated after detection of the minimum duration of 20us of the LOAD pulse at input E/L. With this signal output F_RESET switches over to high level status. Status changeover of output RESET for the low level is performed either by means of the fall edge of the LOAD pulse at E/L input or after comparator option { output COMP_OUT=0 }

By the fall edge F_RESET, the control signal RESET_ENB switches over from the high level to low.

VCO is enabled by a signal from output SET_ENB. The oscillator frequency is trimmed by the external elements at outputs VCO_C, VCO_R, VCO_RV and a signal at output VCO_IN. the resistor value VCO_R determines the slope of the curve Y relative to the axis X. and the resistor value VCO_RV sets the shift of this diagram curve. the oscillator output is delivered to the counter input, which generates the signal SET at output SET. Data at input DATA are written into the counter after detection of the pulse LOAD at input E/L with duration 20 us. Simultaneously with the fall edge of the pulse LOAD at input E/L 6...7 periods are generated of VCO enable delay prior to appearance of the high level at output SET. Duration of the pulse SET is set by the generation period and content DATA written into the counter.

Minimum duration of the pulse F_SET constitutes 0 nanoseconds, if the register has the status { D6=0, D5=0, D4=0, D3=0, D2=0, D1=0, D0=0 }

maximum duration constitutes 127 X Tvco for the register status { D6=1, D5=1, D4=1, D3=1, D2=1, D1=1, D0=1 }

By the fall edge of the output signal SET , the control circuit generates the preset signal "r" ASIC-3A becomes preset and after actuation of the multi vibrator block a new cycle of the circuit operation may start. Simultaneously by the signal fall edge SET , the control signals SET_ENB and SYNC_ENB switch over from the high status into the low one.

For the purpose of testing ASIC-3A has an additional pin CONTROL_PAD, signal at input CONTROL_PAD simplifies the counter testing and check of the output SET_ENB. Low level voltage at output CONTROL_PAD or when the pin is disabled. does not affect the circuit performance. With the high level voltage at pin CONTRL_PAD , pin VCO_OUT switches over into the high impedance and delivery of external signals are permitted to the counter cycling (clock) input.

Table 2 : Electrical parameters

Parameters / measurement modes	**Measurement Units**	**Limits Min**	**Limits Max**	**Remarks**
1	2	3	4	5
Operating temperature	Ta Centigrade	-55	+125	****
Storage temperature	Tstg Centigrade	-65	+150	****
Supply voltage	Vcc V	6.0	7.0	****
Standby current (all digital inputs connected GND) Vcc-7 V, Vvcoin=5.2V, Vih (REF)=6.0V, Vil=0V	Iccs mA	-	2.0	**
Low level input voltage , Vcc 6,7 V At inputs DATA and E/L	Vil V	0	3.5	****
High level input voltage , Vcc 6,7 V	Vih , V	6.0	12.5	****
Low level output voltage Vcc=6.0V, Vvcoin=4.2V, Iol=10uA, Vcc=7.0V, Vvcoin=5.2V, Iol=10uA, Vcc=6.0V, Vvcoin=4.2V, Iol=1.6mA, Vcc=7.0V, Vvcoin=5.2V, Iol=1.6mA	Vol, V	 - - - -	 0.1 0.1 0.4 0.4	 ** ** ** **
High level output voltage, to outputs F_SET, F_RESET, SET_ENB, SYNC_ENB, RST_ENB with Vcc=6.0V, Vvcoin=4.2V, Ioh=10uA, Vcc=7.0V, Vvcoin=5.2V, Ioh=10uA, Vcc=6.0V, Vvcoin=4.2V, Ioh=1.6mA, Vcc=7.0V, Vvcoin=5.2V, Ioh=1.6mA	Voh, V	 Vcc-0.1 Vcc-0.1 Vcc-0.4 Vcc-0.4	 - - - -	 ** ** ** **
Low level output voltage for outputs F_SET, F_RESET with Vcc=6.0V , Vvcoin=4.2V , Iol=10mA	Vol, V	-	1.0	**
High level output voltage at outputs F_SET, F_RESET with Vcc=6.0V , Vvcoin=4.2V , Ioh=10mA	Voh, V	Vcc-1.2	-	**
Input current for CL=180 ..., RL=12 k ohm and Vcc=7.0 V including : High level input current with Vih (E/L, DATA) =12.5V	Iih, uA	-100	100	**

Vih (POR, CP, REF, IN)=(Vcc-0.5) V Low level input current with Vil=0V	Iil, uA	-100	100	**
Voltage Controlled Oscillator				
VCO input voltage range at Vcc= 6,7 V	Vcoin, V	0.5	Vcc-1.8	****
Values range Cvco at input VCO_C	Cvco, pF	100	330	****
Values range Rvco at input VCO_R	Rvco, Kohms	10	300	****
Values range Rvcorv at input VCO_RV	Rvcorv, kohm	10	1000	****
VCO local lineraity of transfer characteristic for CL= 180 pF, RL=12 kohm with : Vcc=(6,6.5)V, Vvcoin= (Vcc/2+/- 0.25) V Vcc=(6.5,7)V, Vvcoin= (Vcc/2+/- 0.25) V	Delta f , %	- -	0.4 0.6	** **
Total (maximum) non-linearity of VCO transfer characteristic for CL=180 pF, Rl= 20kohm and with: Vcc=6.5V, vvcoin=0.5V, (o,5+(Vcc-1.8))/2 V, (Vcc-0.18) V	Deltaf max, %	-	1.8	**
VCO range of frequencies for RL=12kohm, Cl=180pF and with: Vcc=7.0V, Vvcoin =(Vcc-1.8) V Vcc=6.0V, Vvcoin=0.5V	Fvco MHz	4 -	- 1	
Frequency variations within temperature range T=(-55 to 125) degree centigrade with Vcc=6.5V, Vcoin=2.8V	%/degree Centigrade	-	0.1	***
Pulse duration at output VCO_OUT	Duty, ns	90	T/2	***
COMPARATOR				
Range of input voltage values at input Comp_IN common mode voltage, Vcc=6,7 V	Vci, V	0	Vcc-2	****
Input shift current including: Low level input current, Vcc=7.0V, Vil(REF_IN)=0 V High level input current , Vcc=7.0V, Vih (REF_IN)=Vcc	 Ibcl, nA Ibch, nA	 - -	 10 10	 ** **
Shift current at input with Vcc=7.0V	Ioc, nA		2	***
Response delay time at output COMP_OUT on influence of TTL level at input COMP_IN Vcc=6.5 V, Ta=(25 +/- 10) degree C, Cl=15pf	Tp, ns	-	200	**
Shift voltage	Vco, mv	-	7	***
Low level output voltage at output COMP_OUT not over with:				

Vcc=6.0V, Vih=0.007V, Vil=0V	Vol, v	-	0.1	**
Vcc=7.0V, Vih=0.007V, Vil=0V		-	0.1	**
Vcc=6.0V, Vih=(vcc-2.0)V, Vil=(Vin-0.007)V		-	0.1	**
Vcc=7.0V, Vih=(vcc-2.0)V, Vil=(Vin-0.007)V		-	0.1	**
High level output voltage at output COMP_OUT not less with:				
Vcc=6.0V, Vih=0.007V, Vil=0V	Voh, V	Vcc-0.1	-	**
Vcc=7.0V, Vih=0.007V, Vil=0V		Vcc-0.1	-	**
Vcc=6.0V, Vih=(vcc-2.0)V, Vil=(Vin-0.007)V		Vcc-0.1	-	**
Vcc=7.0V, Vih=(vcc-2.0)V, Vil=(Vin-0.007)V		Vcc-0.1	-	**

Table 2a : Dynamic Parameters

Parameters / measurement modes	Measurement Units	Limits Min	Limits Max	Remarks
Duration of start pulse SYNC at input DATA	T1, us	8	16	*
Readiness time (set-up) from the moment of delivery of the start pulse SYNC at input DATA	T2, us	16	32	*
Hold time of data bit at input DATA until the appropriate synchropulse at input E/L	T3, ns	100	-	*
Pulse upper shelf duration of the true signal at input E/L (enable time)	T4T, ns	345	-	*
Pulse upper shelf duration of the false signal at input E/L (enable time)	T4F, ns	-	250	*
Pulse lower shelf duration of the true signal at input E/L (disable time)	T5T, ns	600	-	*
Pulse lower shelf duration of the false signal at input E/L (disable time)	T5F, ns	-	250	*
Data true bit duration at input DATA	T11T, ns	600	-	*
Data false bit duration at input DATA	T11F, ns	-	250	*
Duration of command DATA	Td, us	14.4	17.6	*
Pulse duration between the 8th synchro pulse of the data reception and the signal LOAD at input E/L	T6, us	4	10	*
Duration of true pulse LOAD at input E/L	T7T, us	30	-	*
Duration of the false pulse LOAD at input E/l	T7F, us	-	20.145	*
Delay time of the pulse SET at output SET relative to the reverse edge of the pulse LOAD at input E/L	T10, ns	6T fvco	7T fvco +delta t	***
Duration of the pulse RESET	Tr	>=30 us	10c	***
Duration of the pulse SET at SET	Ts, us	0	127T fvco	***
Propagation delay time of the pulse LOAD at input E/L from the input E/L to output RESET	T12, us	20us	30us +250ns	**
Duration of signal set by output SET_OUT , Vcc=6.26V, Vcoin=2.96V, Cvco_c=180pF, Rvco_r=15.87kohm, Rvco_rv=100 kohm	Ts(127), us	38.7	47.3	*****

NOTES

*	ASIC-3A dynamic parameters (time parameters), compliance with which is checked during functional control
**	-Measurement results are identified for each device at Ta=25+/- 10 ^{0}C -Measurement of device parameters at Ta=-55 ^{0}C and Ta=+125 ^{0}C is performed by each delivery lot by sampling, constituting 5% from the lot, subject to one time shipment to buyer. Samples selection is made by the manufactuer's quality assurance service at random after all units of products passed the compliance control at Ta= (25 +/- 10) ^{0}C and are formed into the lot Acceptance number by the sampling control results Ac=0 ; Rejection number by the sampling control results Re=1;
***	Reference parameter
****	Limit modes
*****	- measurement results are identified by each device at Ta=(25 +/- 10) ^{0}C; -measurement results by duration of the signal SET at output SET_OUT, Vcc=6.26V, Vcoin=2.96V, Cvco_c=180 pF, Rvco_r=15.87 kohm, Rvco_rv=100 kohm are registered on information carrier and delivered to buyer with lot of product

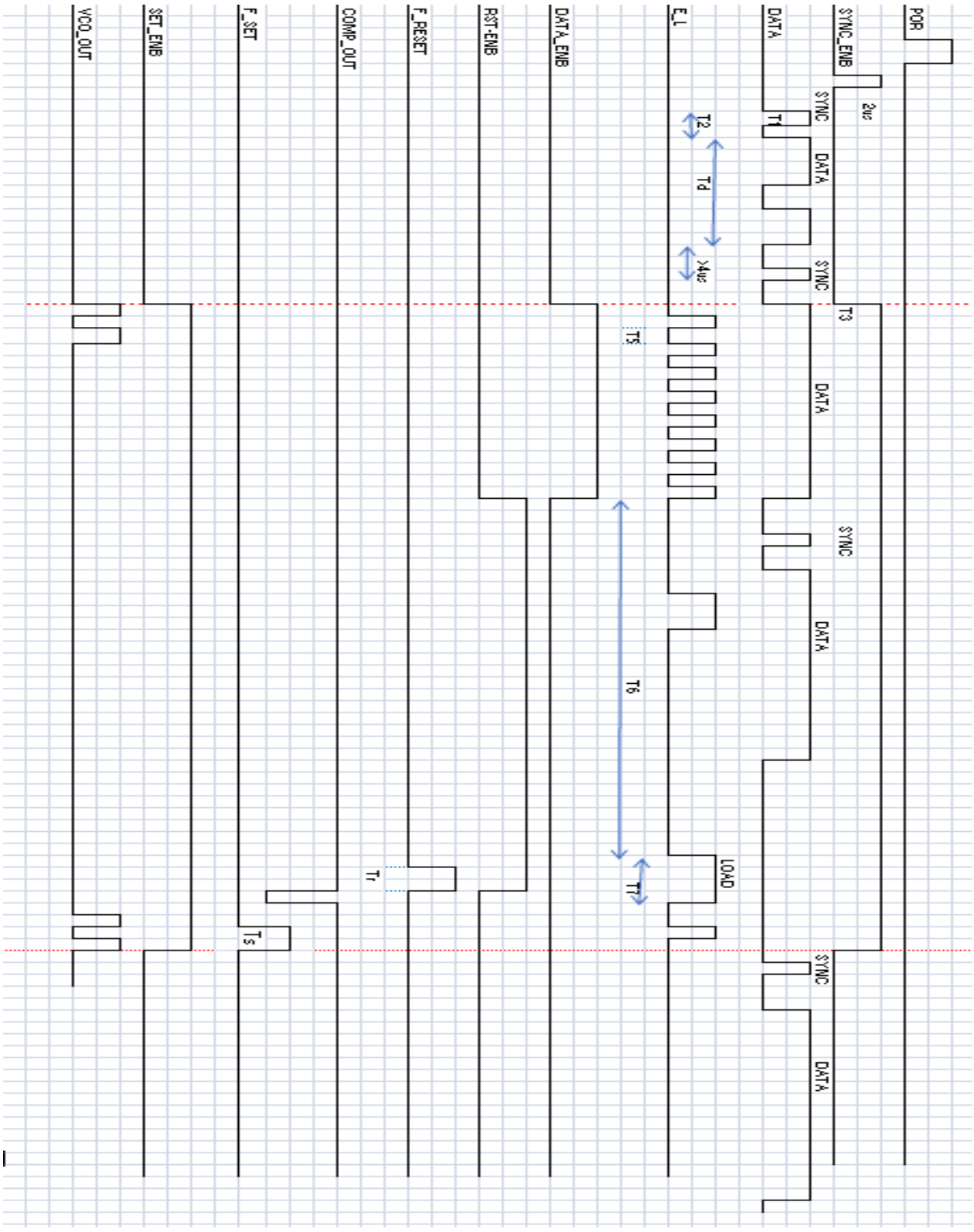
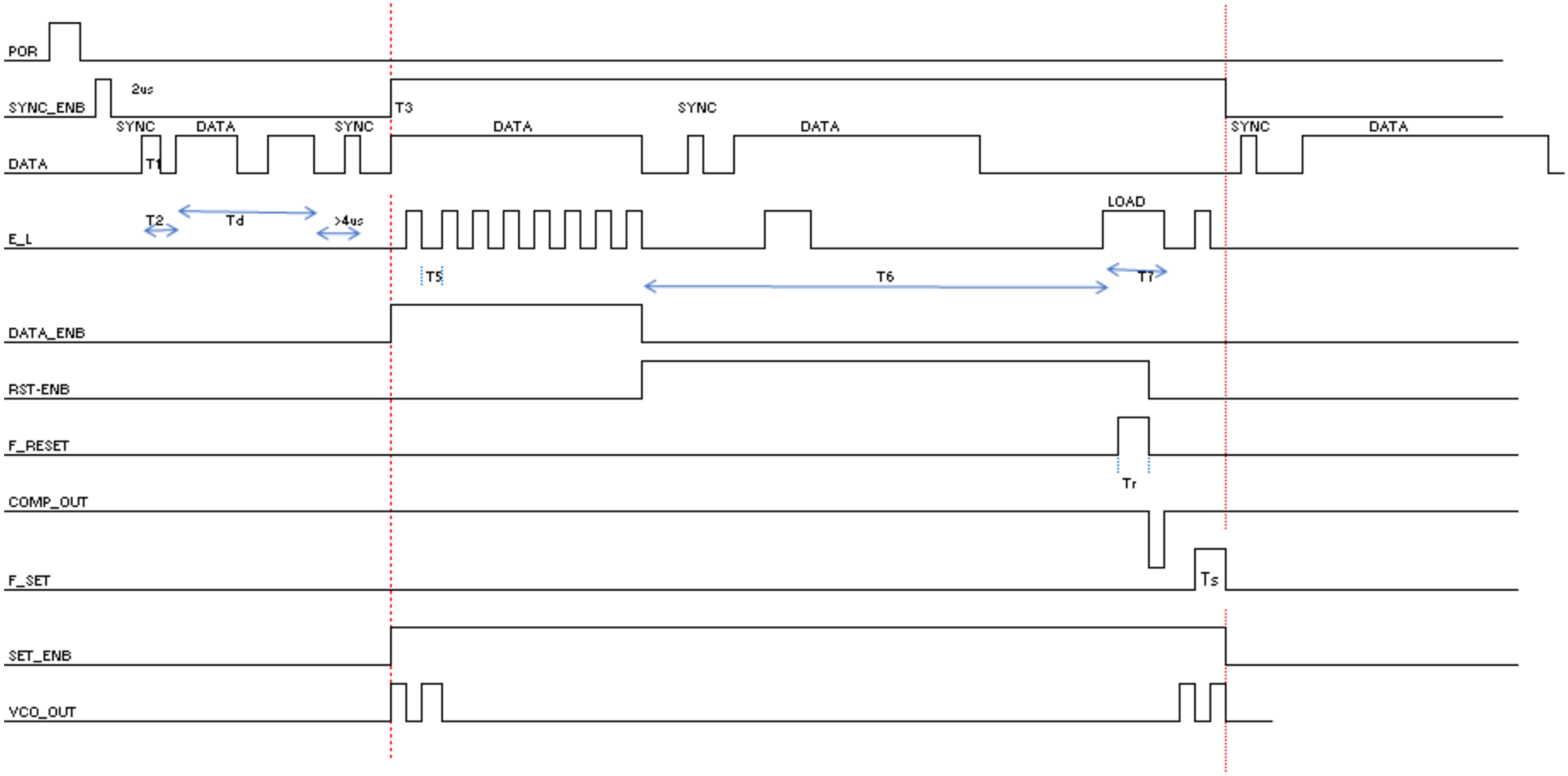


FIGURE 2 - TIMING DIAGRAM


POR
SYNC_ENB
2us
T3
SYNC
DATA
SYNC
DATA
SYNC
DATA
SYNC
DATA
DATA
T1
T2
Td
>4us
E_L
LOAD
T5
T6
T7
DATA_ENB
RST-ENB
F_RESET
Tr
COMP_OUT
F_SET
Ts
SET_ENB
VCO_OUT

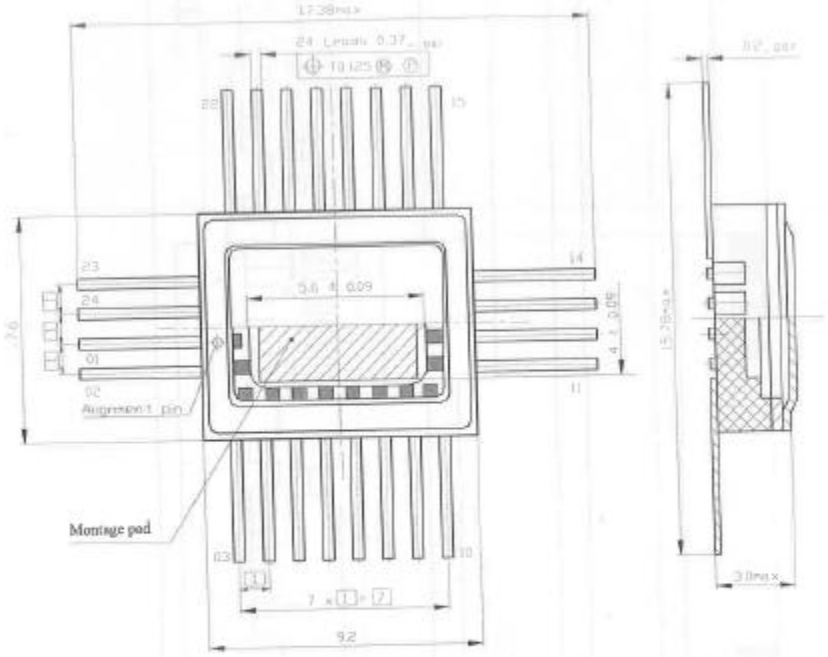


Fig. 3. Dimansional and connection sizes of ASIC-3A in 24-pin metal ceramic package. All sizes are listed in mm

Requirement to ASIC-3 Marking

Marking is applied by the laser engraving method. Marking should be distinct and resistant to solvents. Protective coating on the lid (if required) is applied by the consumer.

Location of the marking information - on the package lid in compliance with fig 4

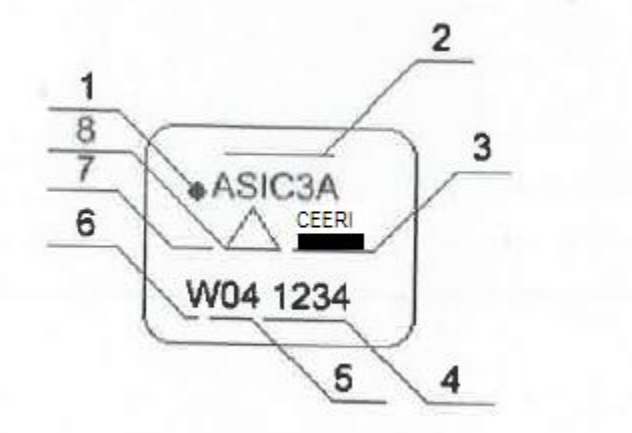


Figure 4 : Example of ASIC-3A marking

Marking composition:

1- sign, indicating that the requirement of radiation hardness are not stipulated.

2- designation of microcircuit (ASIC-3)

3 - name of the company (CEERI)

4 - Variable serial number of microcircuit within a week, corresponding to the test number

5 - variable week number

6 - code of the manufacture

T - FOR 2012	Z - FOR 2018
U - FOR 2013	L- FOR 2019
V - FOR 2014	M- FOR 2020
W - FOR 2015	N- FOR 2021
X - FOR 2016	P- FOR 2022
Y - FOR 2017	

7 - key for the first pin : dot (line) opposite the first pin

8 - sign of sensitivity to static electricity ; even triangle

Note: marking composition and script may be specified at approval by the sides of each lot

The test results of each microcircuit with number and date of manufacture, indicated on the package lid, should comply with the number , indicated on the information carrier (stipulated in the contract)

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