RFIC TECHNOLOGIES

http://www.rficdesign.com
contact ceo@rficdesign.com

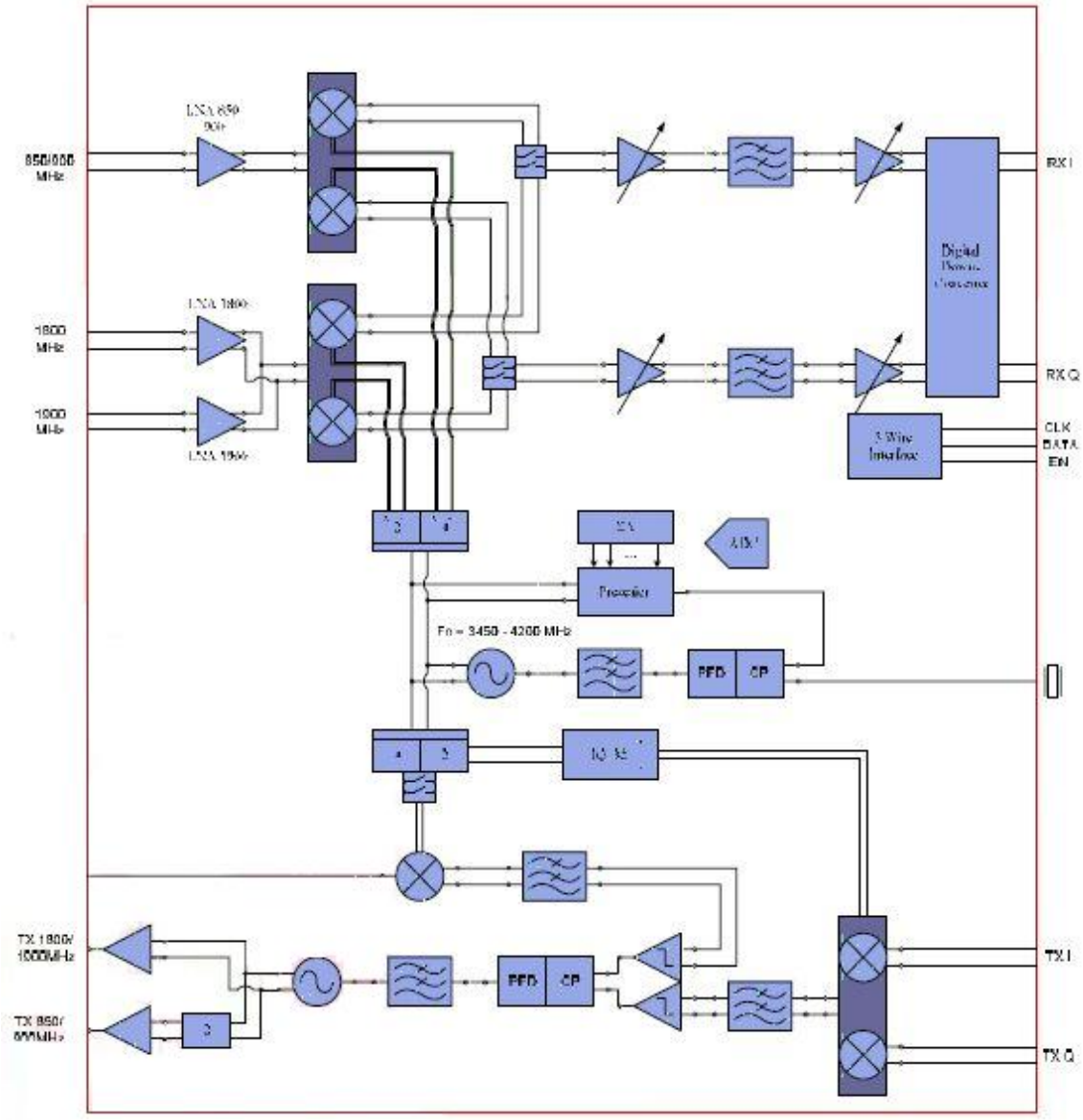
Design of quad band transreceiver

The die size of the transreceiver is 4.2X4.2 mm^2

This is a highly integrated transceiver designed for use in multi-band GSM or GPRS applications. The receiver also supports downlink EDGE. The Transreceiver integrates all sensitive RF components including VCOs and VCO tuning circuitry. It requires a minimum number of external components to complete a GSM radio subsystem. The receive path is based on a digital low-IF (100 kHz) architecture that eliminates the needs for external filters, offers high flexibility and reduces complexity. The Transreceiver receiver includes three differential low noise, gain selectable amplifiers (LNA) followed by quadrature demodulators, programmable low-pass filters and variable gain amplifier that interface to the on-chip digital down-converter. The DC offset of the low-IF section can be removed by using the integrated offset correction loops.

This transceiver presents a universal analog I/Q base band interface, compatible with any supplier's base band subsystem. Alternatively, it can also provide digital RF to base band interfaces for pure digital base band solutions. The TX chain features an I/Q modulator that generates a SSB IF signal which drives a frequency translation loop designed to perform frequency up-conversion with high spectral purity. This loop contains phase-frequency detector, charge pump, offset mixer and a single power VCO that is used to drive both the DCS/PCS band, and through a frequency divider, the GSM band integrated driver amplifiers.

Full chip transreceiver



KEY FEATURES

- VLIF Receiver – Digital Down converter.
- Interface with all existing BB solutions.
- Three Integrated LNAs for Quad Band Support.
- RX Low-IF Filters with tunable bandwidth.
- Gain selectable in 1dB steps.
- Integrated optional DC Offset correction sequencer.
- Offset-PLL Transmitter:
- Reduced Filtering requirements.
- High precision I/Q up-converter.
- Integrated Transmit VCOs.
- Integrated ΣΔ Fractional-N Synthesizer suitable for
- GSM/PCS and GPRS class 12 applications
- Low Cost CMOS Technology.
- 48-pin

TYPICAL APPLICATIONS

- Quad-band support:
- GSM 850
- E-GSM 900
- DCS 1800
- PCS 1900
- GPRS
- EDGE

FUNCTIONAL DESCRIPTION

RECEIVER

The receive path is based on a very low IF architecture which avoids the pitfalls associated with direct conversion while allowing the integration of channel select filters and eliminating the external IF filters required in super heterodyne receivers. Very low-IF receivers are less sensitive to dc offsets and 2nd-order distortion than direct conversion ones and also present higher immunity to device 1/f noise.

This transreceiver includes three differential low noise, gain selectable amplifiers (LNA) each matched to 2 × 50Ohm differential through an external LC matching network. Three gain modes (high, medium and low gain) can be used. Both DCS and PCS bands are supported, while the GSM input supports either the GSM850 or the E-GSM band. Following the LNAs, double balanced mixers convert the RF signal to in-phase (I) and quadrature (Q) signals with an intermediate frequency (IF) of 100kHz. The low-IF signals are DC coupled to a first-order low pass filter and then fed to pair of 6dB step programmable gain amplifiers (3- 21dB). It is followed by 2nd order programmable low-pass filters used for filtering close-in blockers. Finally a first order filter with

programmable gain (5dB gain in 1dB steps) is used to drive a high-resolution on-chip ΣΔ A/D converter (ADC). The ADC (digital) output is directly down converted to base band using a digital 100kHz quadrature signal. Digital filters are used for decimation and channel selection. Benefits of using digital filters include: improved base band filtering with minimum group delay variations, stable performance over process variations, temperature and supply, and low power consumption. To enable compatibility with the existing analog-input base band ICs, a pair of DACs converts the digital signal to the analog domain. Optionally, pure digital signal can be driven directly to the base band IC.

TRANSMITTER

The transmit path is based on the offset PLL architecture, that requires no external filter to attenuate transmitter noise and spurious in the receive bands. An I/Q modulator up converts the differential in phase and quadrature base band signals to generate a single sideband IF signal used as a reference input to the offset PLL. The IF LO is derived from the same Main PLL used for the receive path thus avoiding the use of an additional IF PLL.

The offset PLL consists of a feedback mixer, a phase detector, a loop filter and an integrated power VCO (Transmit VCO). The power VCO that is used to drive both the DCS/PCS band, and through a frequency divider, the GSM band integrated driver amplifiers.

SYNTHESIZER

A Fractional-N phase locked loop (PLL) is used as the Main PLL for both receive and transmit sections of this transreceiver. It includes a Charge Pump with programmable Output Current, a Pre scaler with selectable division range, a fourth order MASH Sigma-Delta Modulator and a 4th order Loop Filter. The LO frequencies are generated by using a fully integrated VCO that requires no external components and operates from 3450MHz to 4200MHz. It is divided by two to cover the DCS/PCS bands and by four to cover the two lower GMS bands. Due to the versatility of the Fractional-N PLL, it can use both 13MHz and 26MHz reference frequencies.