



RFIC System Technologies Private Limited

PROJECT

customer

Author

Version

Date

LDO DESIGN

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initiated

RFIC System Technologies

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Description:

Block diagram

1. system level design and simulation
2. circuit design and simulation
3. layout
4. DRC, LVS
5. post extraction simulation



| | TPS769 | <u>TPS770</u> |
|--------------------------|---|---|
| Iout (Max) (A) | | |
| Output Options | 0.1 | 0.05 |
| Vin (Min) (V) | Adjustable Output Fixed Output | Adjustable Output Fixed Output |
| Vin (Max) (V) | 2.7 | 2.7 |
| Fixed Output Options (V) | 10 | 10 |
| Vout (Min) (V) | 1.2 1.5 1.8 2.5 2.7 2.8 3 3.3 5 | 1.2 1.5 1.8 2.5 2.7 2.8 3 3.3 5 |
| Vout (Max) (V) | 1.2 | 1.2 |
| Iq (Typ) (mA) | 5.5 | 5.5 |
| Vdo (Typ) (mV) | 0.017 | 0.017 |
| Accuracy (%) | 71 | 48 |
| PSRR @ 100KHz (dB) | 3 | 3 |

Specifications:

NOMINAL OPERATING CONDITIONS

| parameters | units | min | typ | max | conditions |
|-------------------------------|-------|-----|-----|-----|---------------------|
| DC VDD voltage | V | | 1.8 | | |
| Analog Voltage | V | | 3.3 | | |
| control voltage "High" | V | | 1.8 | VDD | |
| control voltage "Low" | V | | 0 | 0.3 | |
| operating ambient temperature | C | -40 | | 85 | All operating modes |
| | | | | | |

LDO TECHNICAL PARAMETERS

| parameters | units | min | typ | max | conditions |
|------------------------------|-------|-----|------|-----|------------|
| Vin | V | 1.8 | | 5.5 | |
| Vout | V | | 1.8 | | |
| Dropout voltage | mV | | 150 | | LOAD=300mA |
| Load regulation | % | | 0.5 | | |
| Line regulation | % | | 0.05 | | |
| Standby current | uA | | 0.05 | | Ven=0 |
| PSRR | dB | | 75 | | |
| Thermal shutdown temperature | C | | 165 | | |
| Over current protection | mA | | 150 | | |
| Operating temp | C | -40 | | 80 | |
| Output voltage noise | uVrms | | 200 | | |



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Block Diagram

Chip diagram

Test bench

Circuit design

Simulation results

Layout

Verification results

Conclusion

Reference

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