



RFIC System Technologies Private Limited

PROJECT

customer

Author

Version

Date

LDO DESIGN

Suchitav Khadanga

initiated

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RFIC System Technologies

401, Green Castle, ASM Road, Ulsoor, Bangalore, India-560042

Email: admin@rficdesign.com phone: 91-80-25300747 <http://www.rficdesign.com>

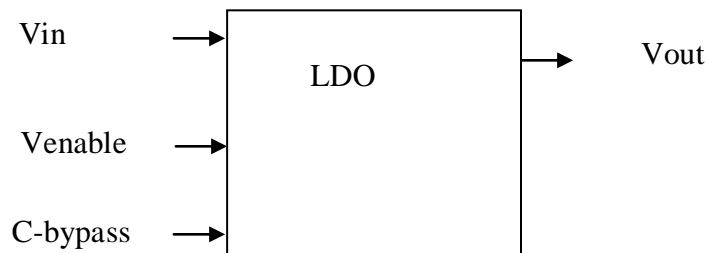
Description:

This LDO-Low dropout regulator is suitable for noise sensitive applications such as Phase Locked Loops, Oscillators, Frequency Synthesizers, Low Noise Amplifiers and other Precision Instrumentation require very clean power supplies.

Special feature

Ultra-Low Quiescent Current, Ultra-Low Noise

Block diagram



- Vout load capacitor is 1uF (external)
- C-bypass is 0.01 uF (external)
- Vin 2.0 to 5.5 V
- Vout 1.8V
- Venable digital input
- Max Dropout voltage 150mV



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1. system level design and simulation
2. circuit design and simulation
3. layout
4. DRC, LVS
5. post extraction simulation

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Specifications:

NOMINAL OPERATING CONDITIONS

parameters	units	min	typ	max	conditions
DC VDD voltage	V		1.8		
Analog Voltage	V		3.3		
control voltage "High"	V		1.8	VDD	
control voltage "Low"	V		0	0.3	
operating ambient temperature	C	-40		85	All operating modes

LDO TECHNICAL PARAMETERS

parameters	units	min	typ	max	conditions
Vin	V	2.0		5.5	
Vout	V		1.8		
Dropout voltage	mV		150		LOAD=300mA
Load regulation	%		0.5		
Line regulation	%		0.05		
Standby current	uA		0.05		Ven=0
PSRR	dB		75		
Thermal shutdown temperature	C		165		
Over current protection	mA		150		
Operating temp	C	-40		80	
Output voltage noise	uVrms		200		



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Block Diagram

Chip diagram

Test bench

Circuit design

Simulation results

Layout

Verification results

Conclusion

Reference

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